

EDN[®]

Troubleshooting
analog circuits—Part 8

Real-time kernels
for single-chip μ Ps

Keeping your PC data safe

Buscon/89 preview

10/30/89

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



Nonvolatile memories let
applications weather any storm

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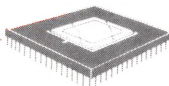
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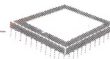
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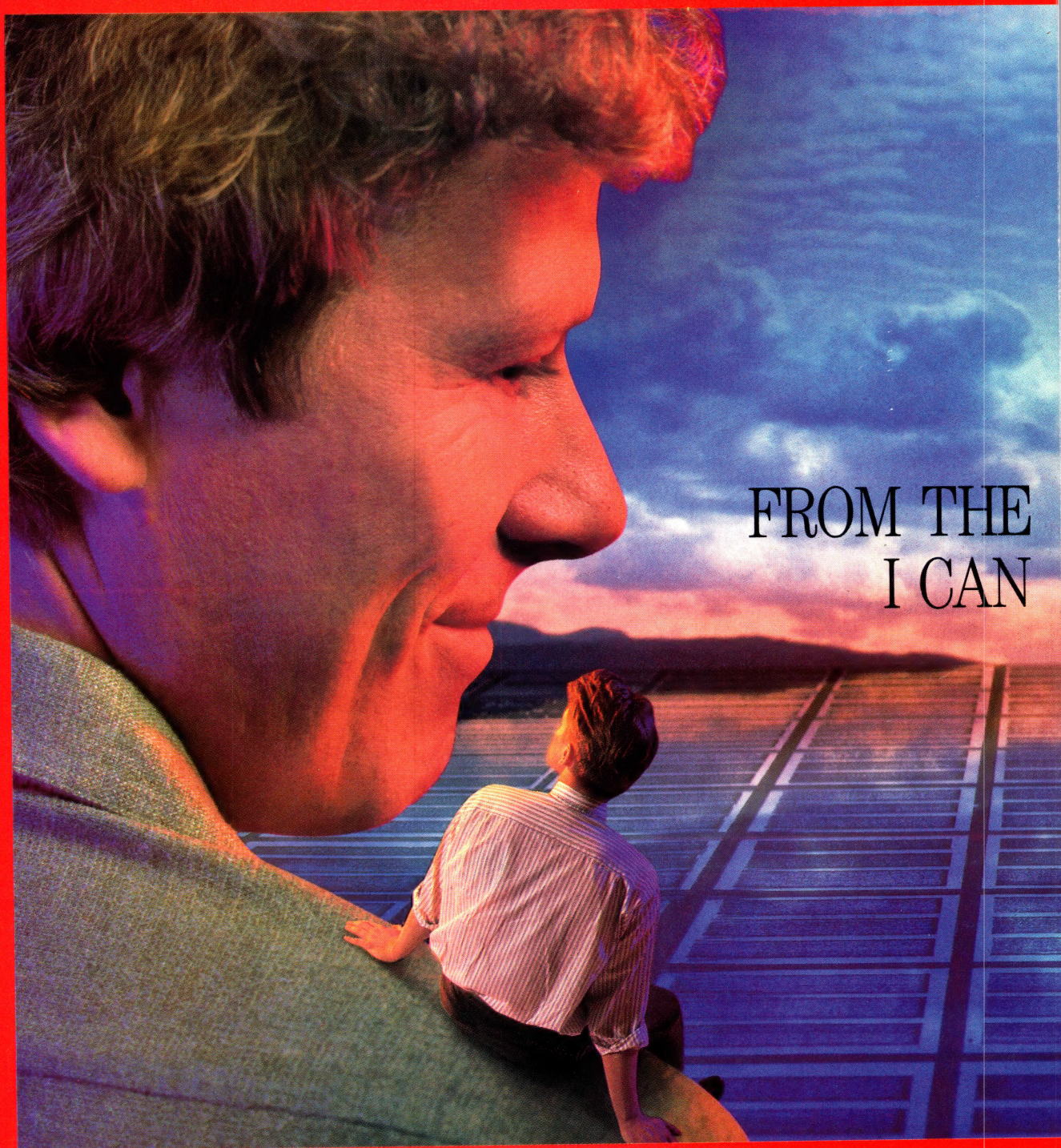
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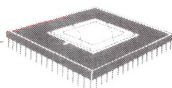


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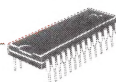
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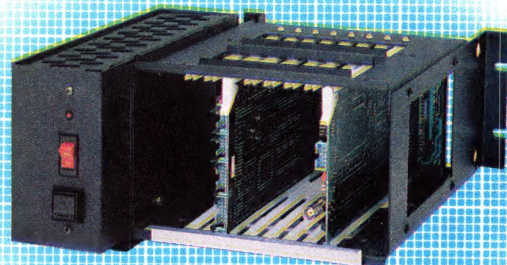
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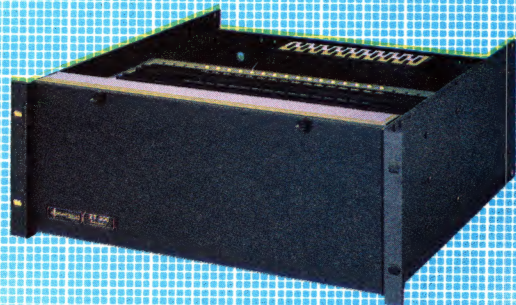
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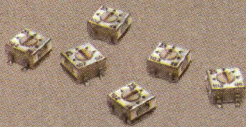
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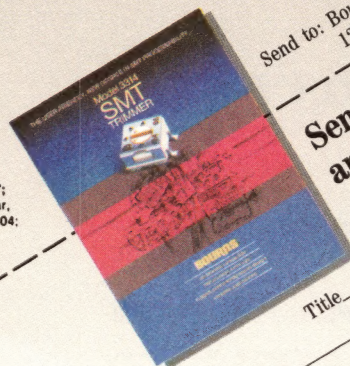
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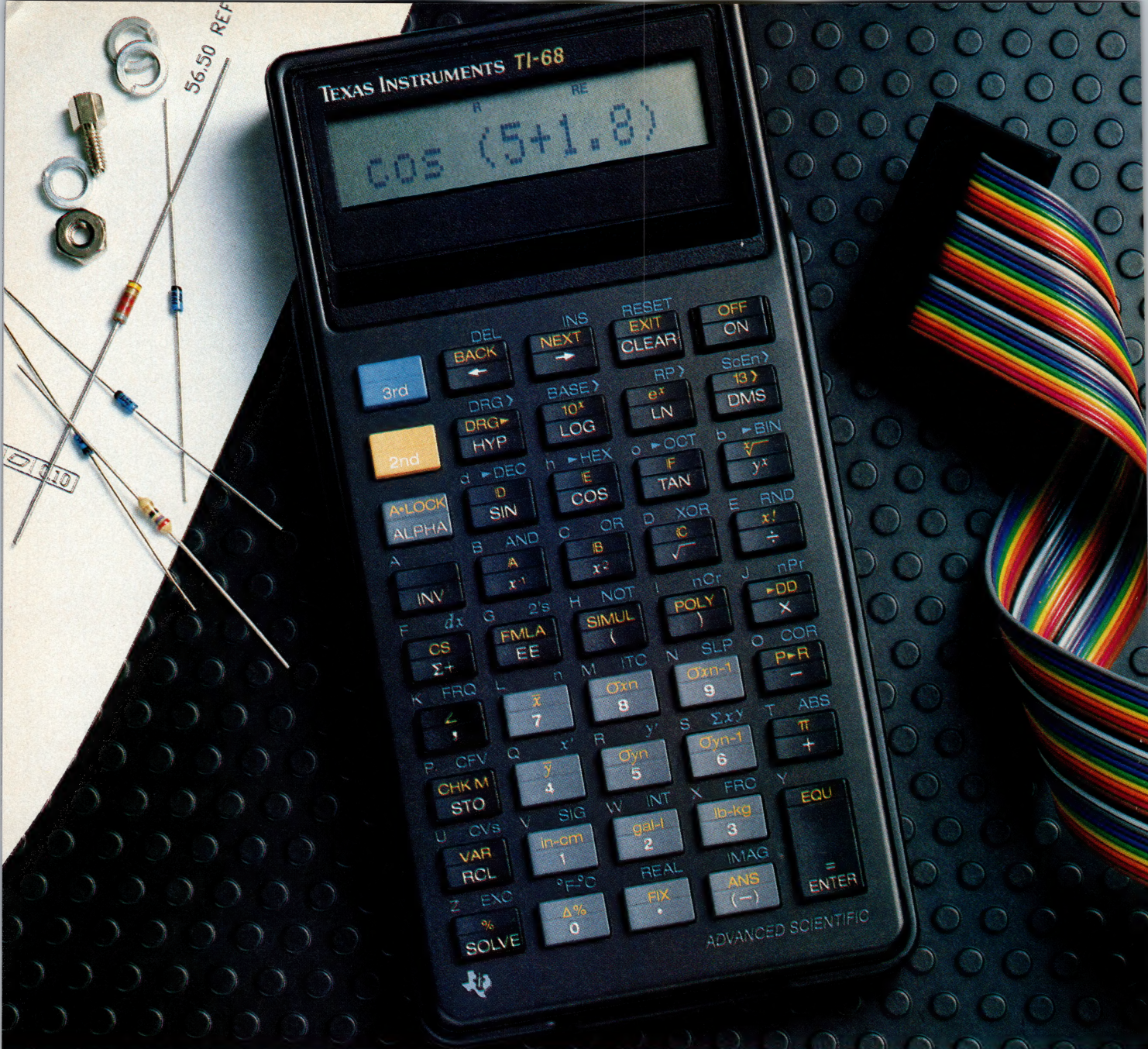
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TEXAS
INSTRUMENTS



On the cover: Because of the enormous variety of nonvolatile memories on the market, you'll have no trouble selecting a device that will satisfy all of your cost, flexibility, and performance requirements. See the Special Report, beginning on pg 94. (Photo courtesy Cypress Semiconductor)

SPECIAL REPORT

Nonvolatile memories

94

With such a wide range of nonvolatile-memory types and performance capabilities available, it can be a daunting task to find the right one for your application. As a result, it helps to have a good idea of what your choices are, so you can avoid some of the confusion about what a memory can or cannot do.—*Michael C Markowitz, Associate Editor*

DESIGN FEATURES

Proper output decoupling maximizes power-supply operation

117

The decoupling technique presented here lets you develop an optimum supply-load decoupling network. You need to know only two values—the supply's output impedance and the capacitor's impedance characteristics—to solve noise problems without causing oscillation.

—*Steven C Hageman, Callex Mfg Co Inc*

Troubleshooting analog circuits Part 8

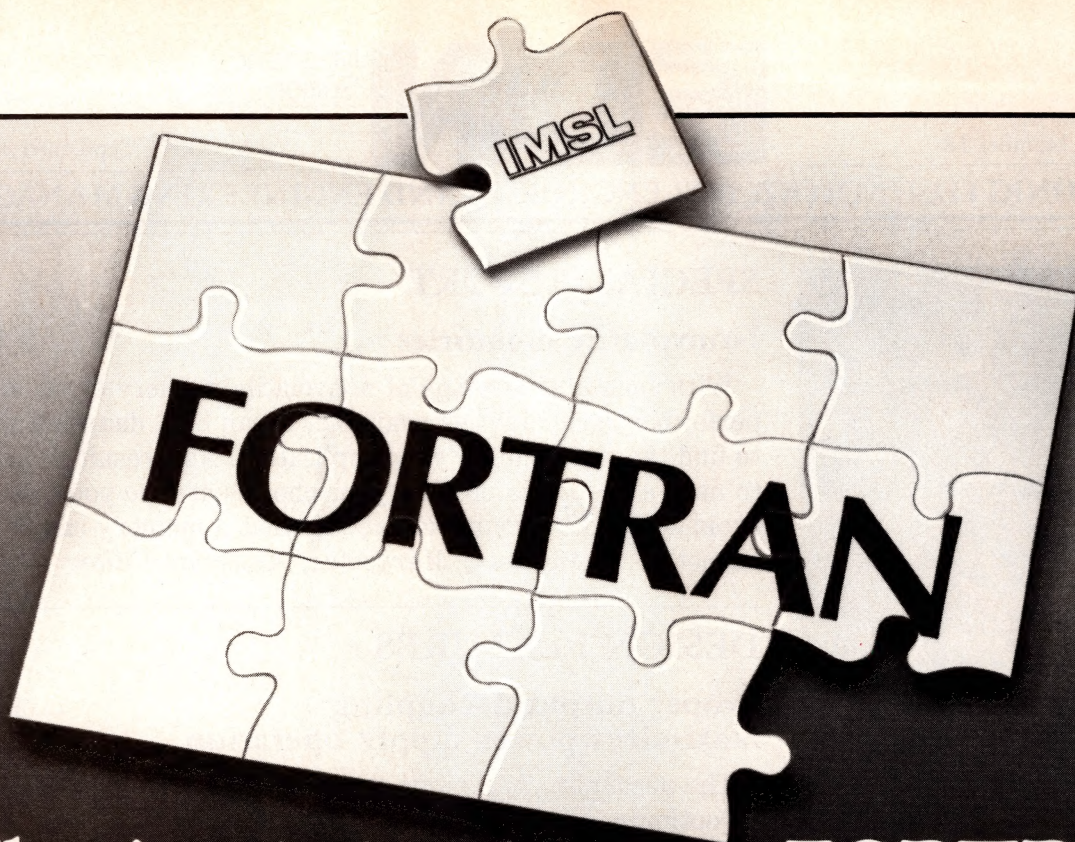
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External components often determine an op amp's performance—that's why Bob spent the previous seven parts of this series discussing them. But op amps aren't trouble-free: Oscillations and noise are two common problems. You'll have similar trouble with buffers and comparators, which Bob will discuss in part nine.

—*Robert A Pease, National Semiconductor Corp*

Continued on page 7

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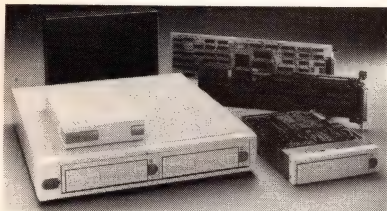
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To keep your data secure, you can use removable drives. Or you can check out the numerous other methods that will protect your sensitive information (pg 61).

TECHNOLOGY UPDATES

Hardware and software keep your PC data safe

61

Even companies that don't handle classified information must protect the data on which their business depends, and they must strike a balance between doing nothing (which leaves them open to disaster) or installing such stringent security measures that productivity suffers (which may result in users trying to ignore these measures, or merely being sloppy about observing them).

—Chris Terry, Associate Editor

Real-time kernels scarce for single-chip μ Ps

79

Unfortunately, even though a wide variety of third-party, real-time kernels and operating systems are available for standard μ Ps, far fewer formal, real-time tools are available for single-chip μ Ps.—Charles H Small, Associate Editor

Keep up with bus technology at Buscon

88

Buscon East moves from New York last year to the Boston area this month, bringing with it its traditional grab bag of sessions and product exhibits that will bring you up to date in the field of computer-bus technology.

—Joan Morrow, Assistant Managing Editor

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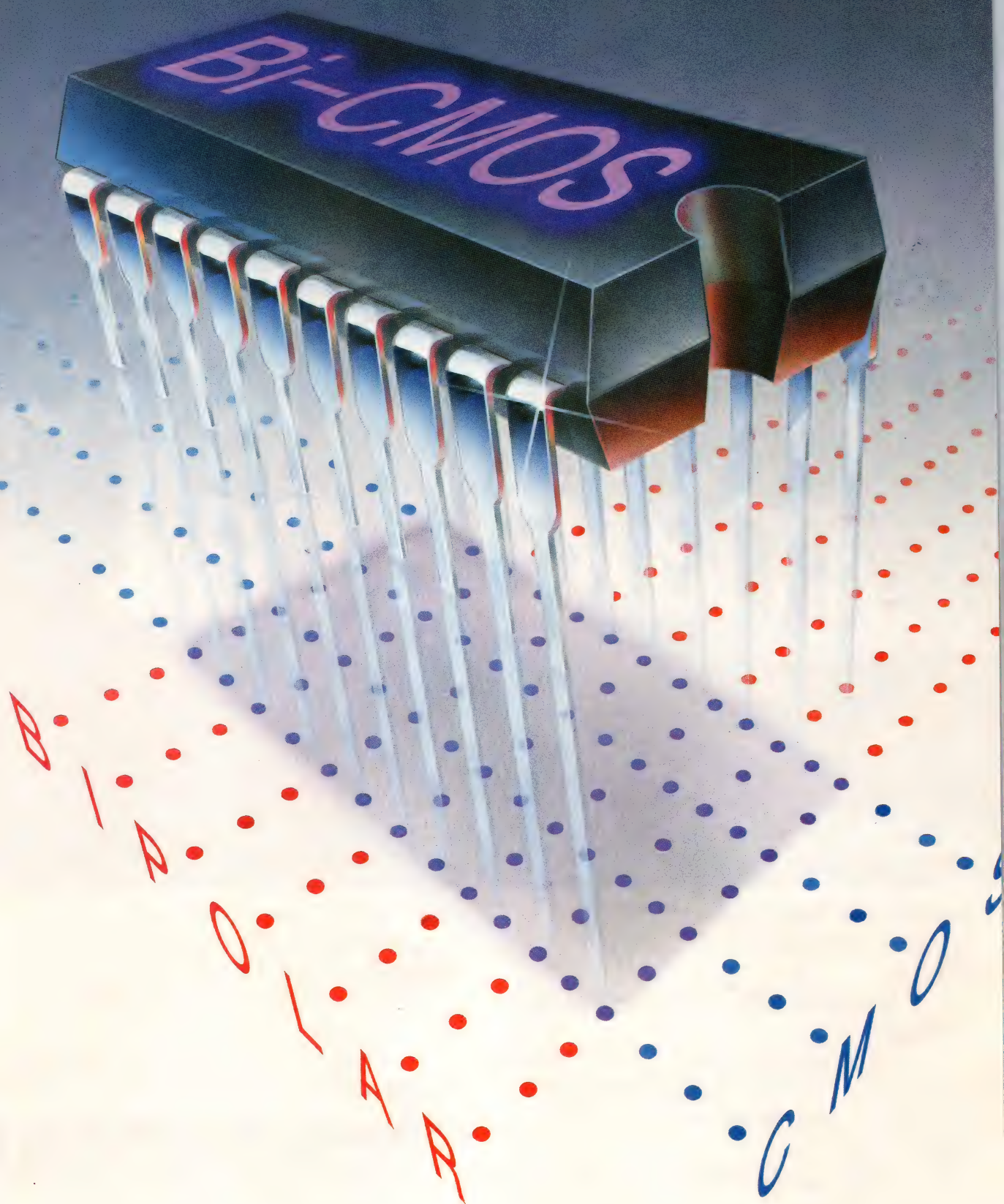
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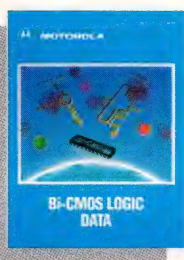
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SELECTION GUIDE

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Resolution	12 Bits	12 Bits	12 Bits	12 Bits
Power Dissipation (mW)	55	400	65	65
Power Supply Voltage	+5 V	+5 V, ± 12 V or ± 15 V	+15 V or ± 15 V	+15 V or ± 15 V
Bus Interface	Parallel	Nibble, Byte, Parallel	Parallel	Byte
Comments	12-Bit DACPORT™	Four DACs, Multiplying Capability	12-Bit DACPORT	12-Bit DACPORT

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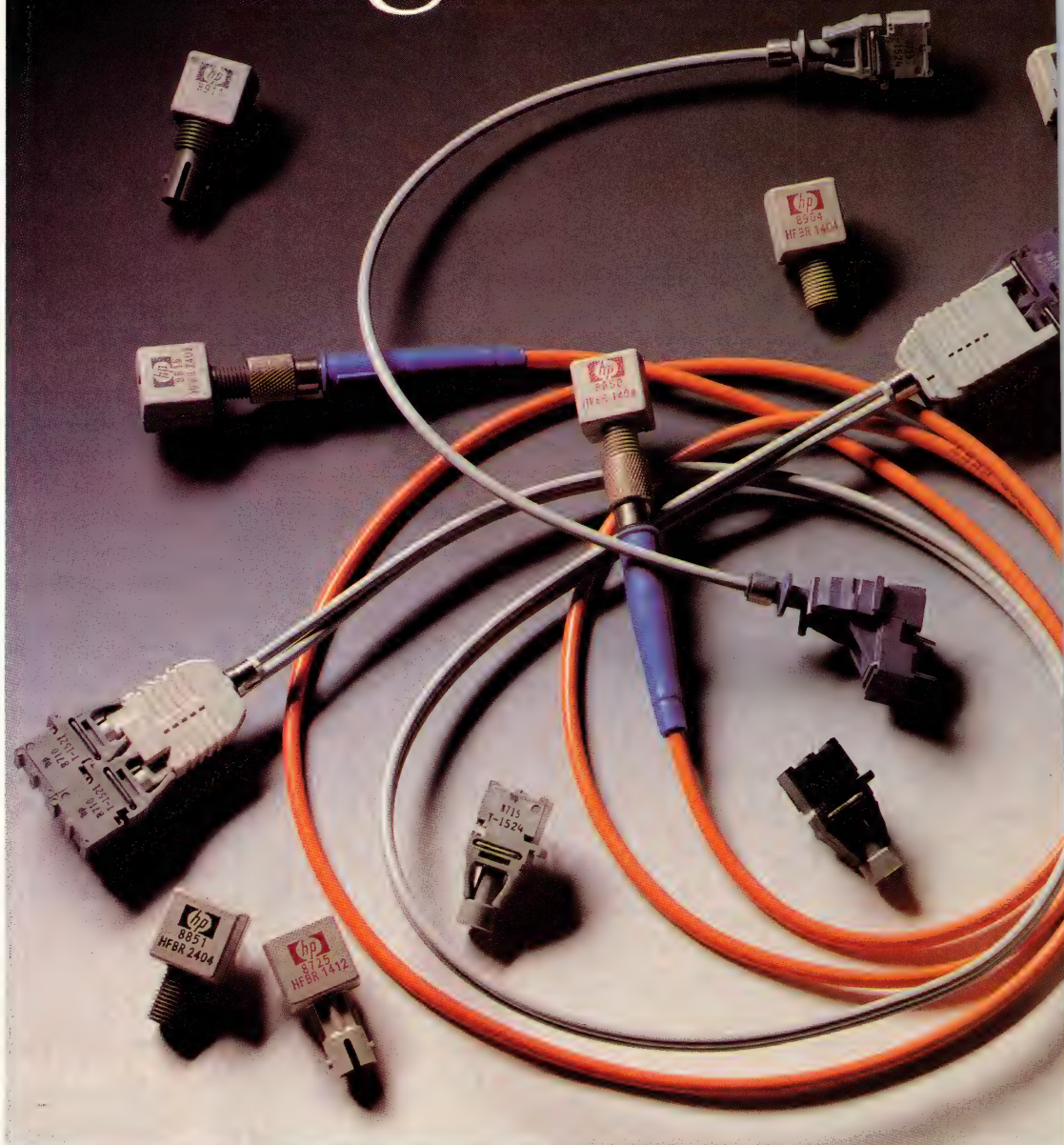
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NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

COMPANY PROPOSES 32-BIT VERSION OF STD BUS

The STD Bus's 4.5×6.5-in. size and rugged board-mounting scheme make it a good candidate for industrial and medical equipment. However, the 8-bit bus runs out of steam in sophisticated systems requiring increasing amounts of processing and computational power. Yet when faced with the prospect of moving to a wider bus, such as Nubus or Futurebus, designers of STD Bus-based systems are reluctant to give up their experience using the STD Bus's hardware and software.

Ziatech Corp (San Luis Obispo, CA, (805) 541-0488) has proposed a 32-bit-wide bus, the STD 32, that's compatible with the old 8-bit cards. The company proposes that a second row of connector pads be added between the relatively widely spaced pads that now exist. This technique is similar to that used by the EISA bus, the 32-bit extension to the 16-bit PC/AT bus. Ziatech has delivered the specification to the STD Bus Manufacturers Group. The company will be announcing products based on this new bus in September.—Margery Conner

CHIP SET ACCOMMODATES ALL 80286 AND 80386 μ Ps

IBM PC-compatible chip sets have yet to saturate the market, according to Via Technologies Inc (Fremont, CA, (415) 651-2796). The company says that you can use a set of its four basic Flexset ICs regardless of the type of 80286 or 80386 device or the speed grade you choose to use. However, in the case of the 80386 μ P, you'll need a different memory-controller chip and an extra data-bus buffer. Prices for the 4-chip set are less than \$40 in 10,000-set quantities. Beyond the basic chips, the company also offers complete mother boards for the 32-bit 80386 and the 16-bit 80386SX μ P ICs. By starting your design with a complete mother board that incorporates the chip set, you can concentrate on your application and not on first testing and debugging your CPU card or mother board. The FlexAT/386SXP mother board costs \$1200, and the FlexAT/386DXP mother board costs \$1300. Delivery is six weeks ARO. Both boards can accept either a Weitek or an Intel math coprocessor chip. The company can also supply complete pc-board layout information in the form of negatives or net lists for CAE use.—Jon Titus

ASIC VERIFIER SPORTS MIXED-SIGNAL CAPABILITY

Because most ASICs designed so far have been purely digital, engineers needing to verify the design of mixed-signal ASICs have been left to their own devices. However, Integrated Measurement Systems (IMS), a subsidiary of Valid (Beaverton, OR, (503) 626-7117, FAX 503-644-6769) has announced a \$60,000 to \$120,000 mixed-signal ASIC verification system. If you own one of IMS's LogicMaster XL systems, you can upgrade it to include the mixed-mode capability. At the heart of the hardware are a 12-line×16-pin relay matrix characterized to 500 MHz and a fixturing scheme that obviates most hand wiring. The system, which has a noise floor of 22 μ V p-p, uses an 80386-based PC and accommodates IEEE-488 instruments of your choice. To keep the code compact, the software, which runs under MS-Windows, lacks some of the features of instrument-control packages intended for more general application. For example, it won't display "virtual" instrument panels on the computer's monitor, but it will let you integrate instrument-control procedures into device-test programs.—Dan Strassberg

NEWS BREAKS

SERIAL EEPROM STORES 1k BYTES AND RUNS ON 3V

For less than \$2 (1000) you can put 1k byte of EEPROM in your next design with the XL93CS46 from Exel Microelectronics Inc (San Jose, CA, (408) 432-0500). Packaged in an 8-pin DIP, the memory device runs on both 5 and 3V power supplies and draws only 2 μ A when running on 3V in its standby mode. Internally, the serial EEPROM stores data in 64 16-bit registers, and you can store information in these nonvolatile registers as many as 100,000 times. You can safeguard a variable number of the registers from being overwritten by using the chip's protect register.

—Steven H Leibson

FIRST AUTOMATIC PARALLELIZING ADA COMPILER HITS MARKET

If you plan to use the Ada programming language in your next project, you should know that an Ada compiler that automatically creates parallel, parallel/vector, and nested parallel loops has passed the US government's Ada Compiler Validation Capability test. Prices for Convex Computer Corp's (Richardson, TX, (214) 497-4226) Ada version 1.1 start at \$30,000. Designed to run on the company's parallel-processing computers, a \$50,000 version of this compiler includes a task-spreading capability. This capability lets your Ada program run on multiple CPUs, thus taking advantage of the Convex's C200 computer series' automatic self-allocating processor mechanism. The Ada debugger supports both parallel and multitasking applications.

—J D Mosley

ASIC VERIFICATION SYSTEM SUPPORTS FULL SCAN TESTING

By adding a scan test module to the XL Logic Master series of ASIC-verification testers from Integrated Measurement Systems (Beaverton, OR, (503) 626-7117), you can implement a wide range of scan test methods at speeds as fast as 60 MHz. Scan test options supported by the module include the IEEE P1149.1 standard proposed by the Joint Test Action Group (JTAG), scan path, scan set, random-access scan, boundary scan, and level-sensitive scan design (LSSD). Each scan module supports four input/output channels with 1M data bits behind each channel. To increase memory depth, you can multiplex data to one or two channels, and you can expand a system to include as many as seven modules for wider or deeper scan channels.

The system maintains full flexibility when using the scan test module, thus letting you perform full functional, parametric, and scan testing without having to change device fixtures. All channels can be used for clock, data, or control functions, and you can clock serial and parallel vectors at different rates. Software included with the module lets you reformat serial data into pattern displays for easy viewing. The scan test module will be available in the fourth quarter of 1989 for \$33,000.

—Doug Conner

T/H BUFFER ACQUIRES SIGNALS TO 0.01% IN 25 NSEC

If you need to freeze high-speed analog signals for accurate digitization, the CLC942 from Comlinear Corp (Fort Collins, CO, (303) 226-0500) features a 25-nsec hold-to-track acquisition time, settling to within 0.01% of the input signal within that period. The company claims that this speed is fast enough to allow 12-bit digitization of signals at 20 MHz. The industrial version of the track-and-hold buffer with an operating-temperature range of -25 to +85°C costs \$139 (100).

—Steven H Leibson

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NEWS BREAKS

SCSI CHIP INTEGRATES CORE μ P AND DMA CONTROLLER

The SIOP386 SCSI IC from NCR (Colorado Springs, CO, (800) 525-2252) includes interface circuitry, a 32-bit DMA controller, and a user-programmable μ P core. The basic SCSI-interface circuitry provides register-level access to the interface signals, but the interface can also be controlled directly by the processor or remotely via the DMA channel. In particular, the SCSI chip targets applications in IBM-compatible PCs, both on host adapters and directly integrated in mother boards. The modular design of the chip will enable the company to offer customized versions for other computer types as well as updates of the chip that are compatible with new versions of the SCSI spec. The IC costs \$48.65 (1000).—Maury Wright

RS-232C TRANSCEIVER IC STEALS CURRENT FROM HOST

The DS1275 line-powered transceiver from Dallas Semiconductor (Dallas, TX, (214) 450-0400) permits battery-operated equipment to reduce the current drain that occurs when communicating with personal computers by siphoning power from the host computer's RS-232C signals. To communicate via RS-232C serial lines, you previously had to add voltage-conversion circuitry to your design to convert the battery voltage to ± 10 V. However, the DS1275 takes advantage of the fact that the host computer already generates the required voltage, thus reducing the portable device's current requirements by an order of magnitude. And when your portable unit is not transmitting data, this IC draws no battery current at all. The DS1275 sells for \$1.73 (5000) and comes in an 8-pin DIP or a surface-mount package.—J D Mosley

STD BUS MODULE INCLUDES COMPLETE PC/XT-COMPATIBLE PC

Computer Dynamics (Greer, SC, (803) 877-8700) now offers the CPU-XT single-slot, STD Bus module, which includes all of the functions typically found in an IBM PC/XT computer except disk drives and a power supply. The module can host an Intel 8088 or NEC V20 μ P at clock speeds as fast as 9.54 MHz. In addition, the card includes 128k bytes of EPROM, 256k to 640k bytes of RAM, a keyboard interface, a timer, and a battery-backed clock calendar. Furthermore, the product includes a standard floppy/Winchester disk controller and a graphics controller. Target markets for the module include applications in OEM enclosures and rugged industrial applications. The CPU-XT costs \$995.—Maury Wright

80386 2-WAY, SET-ASSOCIATIVE MEMORIES SHRINK CHIP COUNT

Two cache memory ICs introduced by Sony (Cypress, CA, (714) 229-4197) and Saratoga Semiconductor (Sunnyvale, CA, (408) 522-7500) can reduce the chip count and increase the speed of 80386 cache memories running at 16 to 33 MHz. Both chips reduce the number of ICs needed to implement a 32k-byte, 2-way, set-associative memory from over 20 to just two by combining the memory ICs and address latches. Sony's chip, the CXK7701, includes a bus transceiver and is available with access times of 30, 35, 45, and 55 nsec. Prices start at \$49.50. Saratoga's SSM51186, which has a similar architecture, has an access time as fast as 20 nsec. Prices start at \$69.70.—Margery Conner

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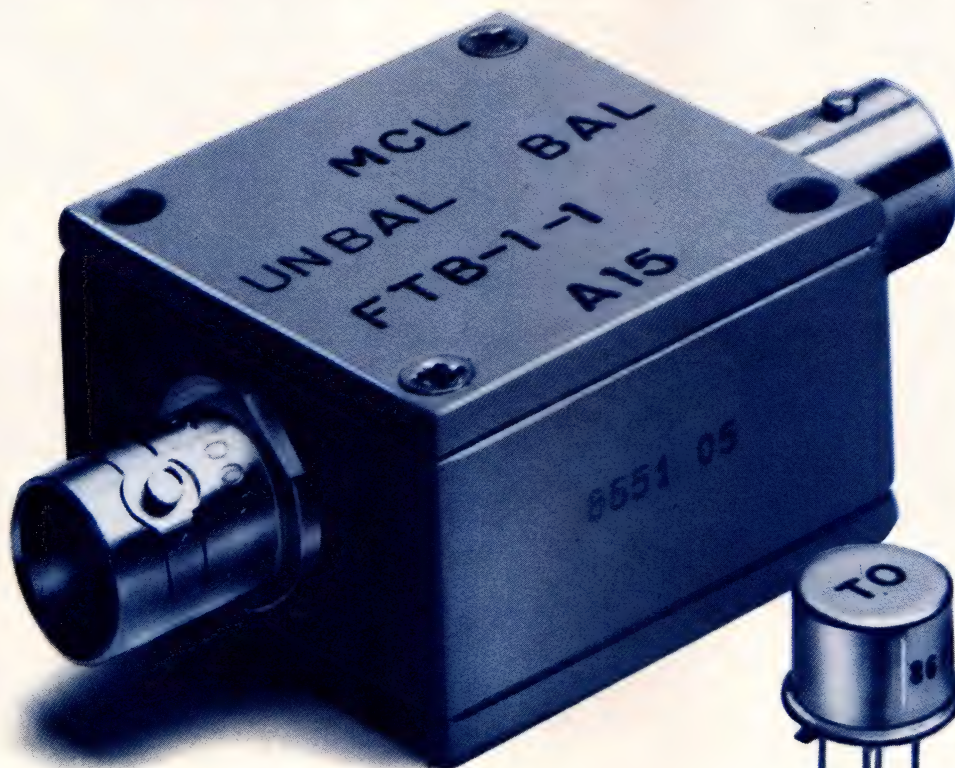
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Pass Band (MHz) start, max.			41	90	133	185	225	290	395	500	600	700	780	910	1000
end, min.			200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
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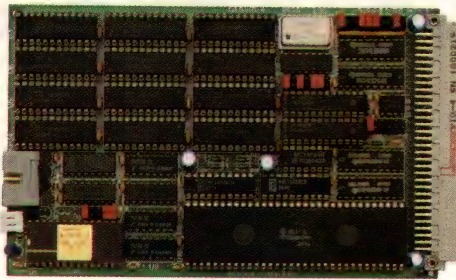
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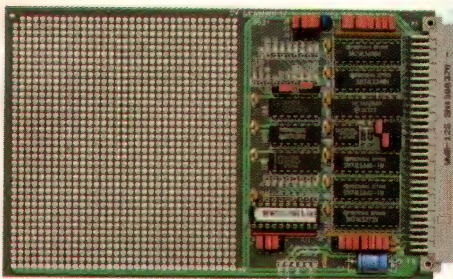
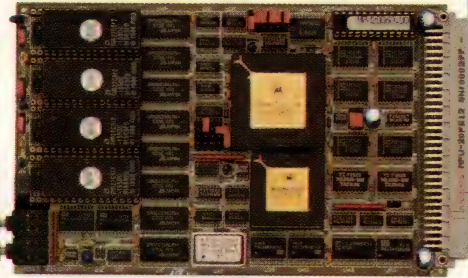
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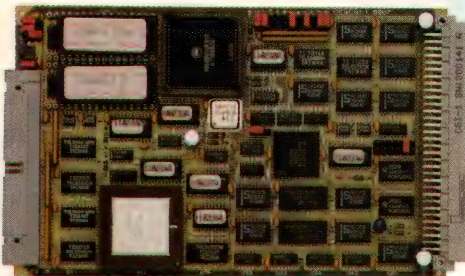
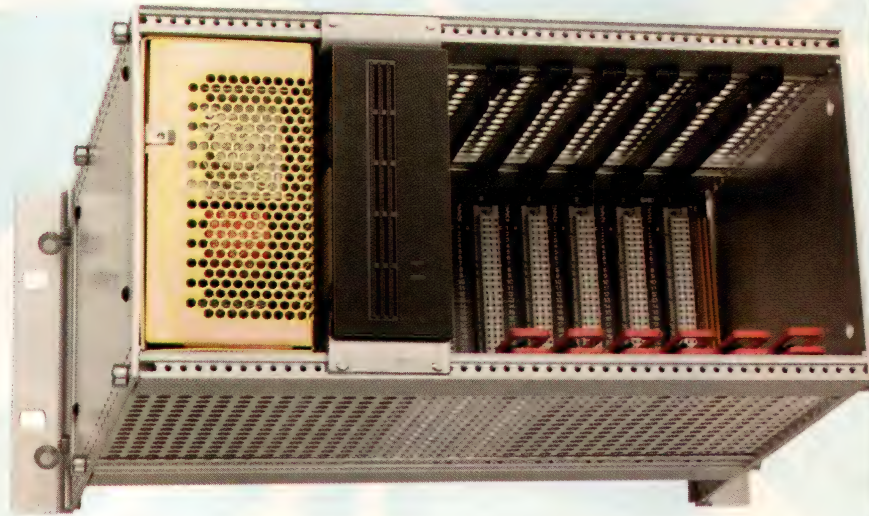
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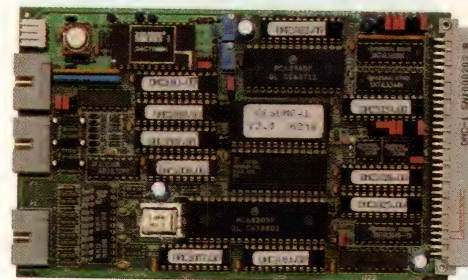
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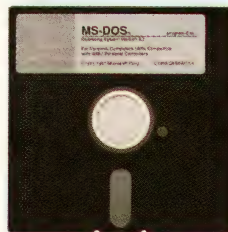
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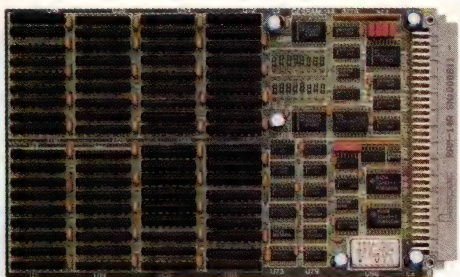
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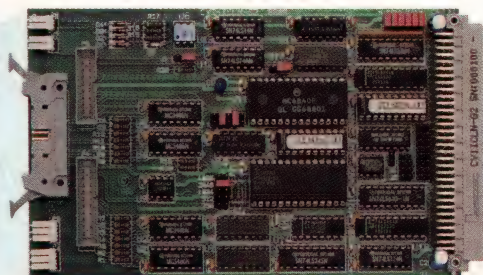
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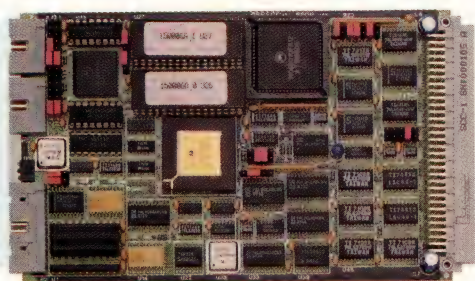
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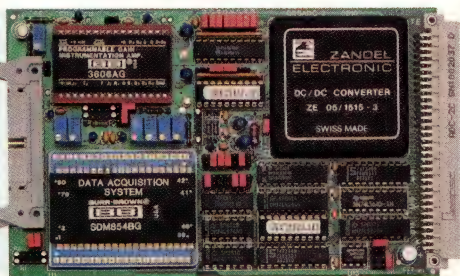
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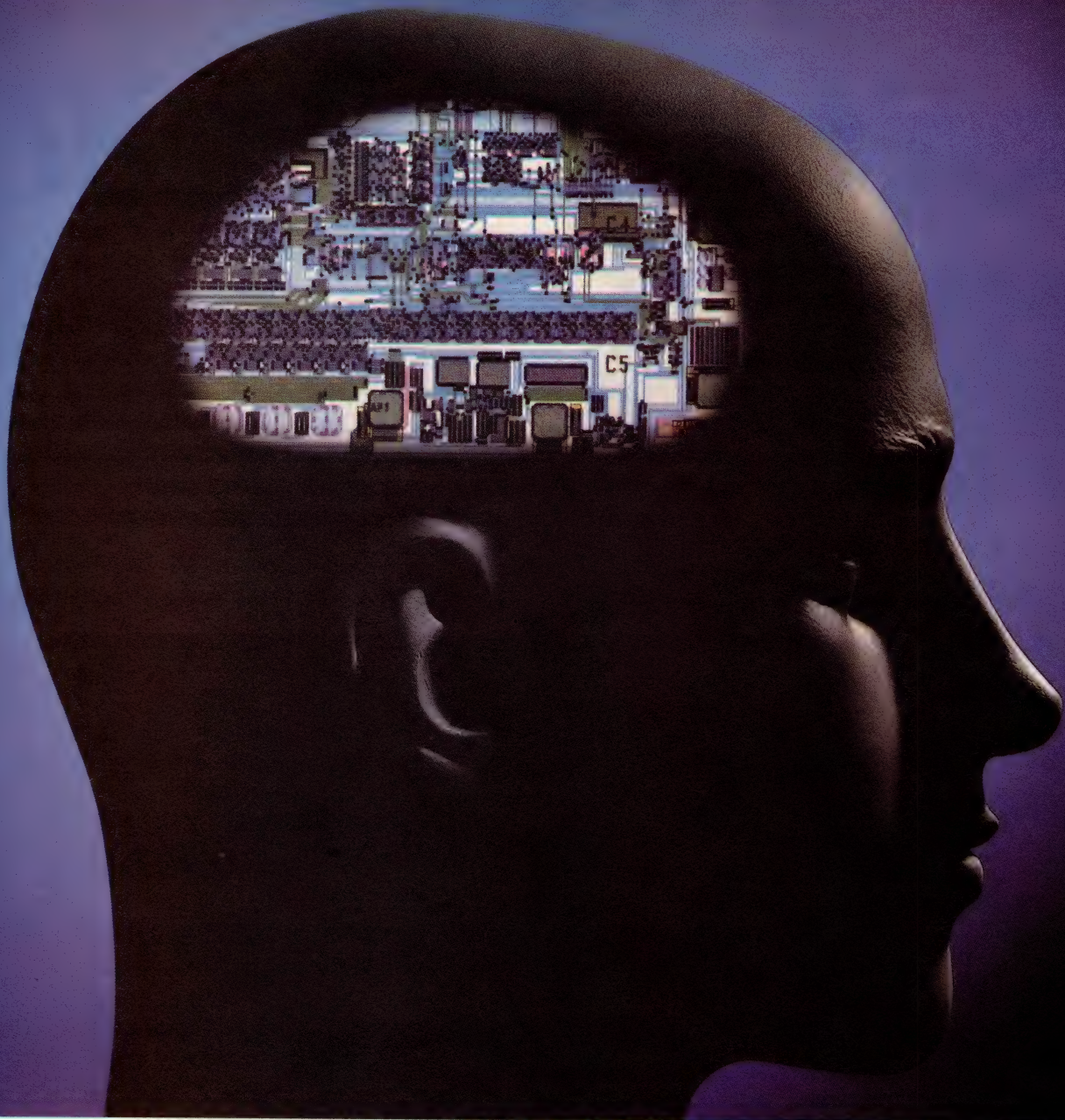
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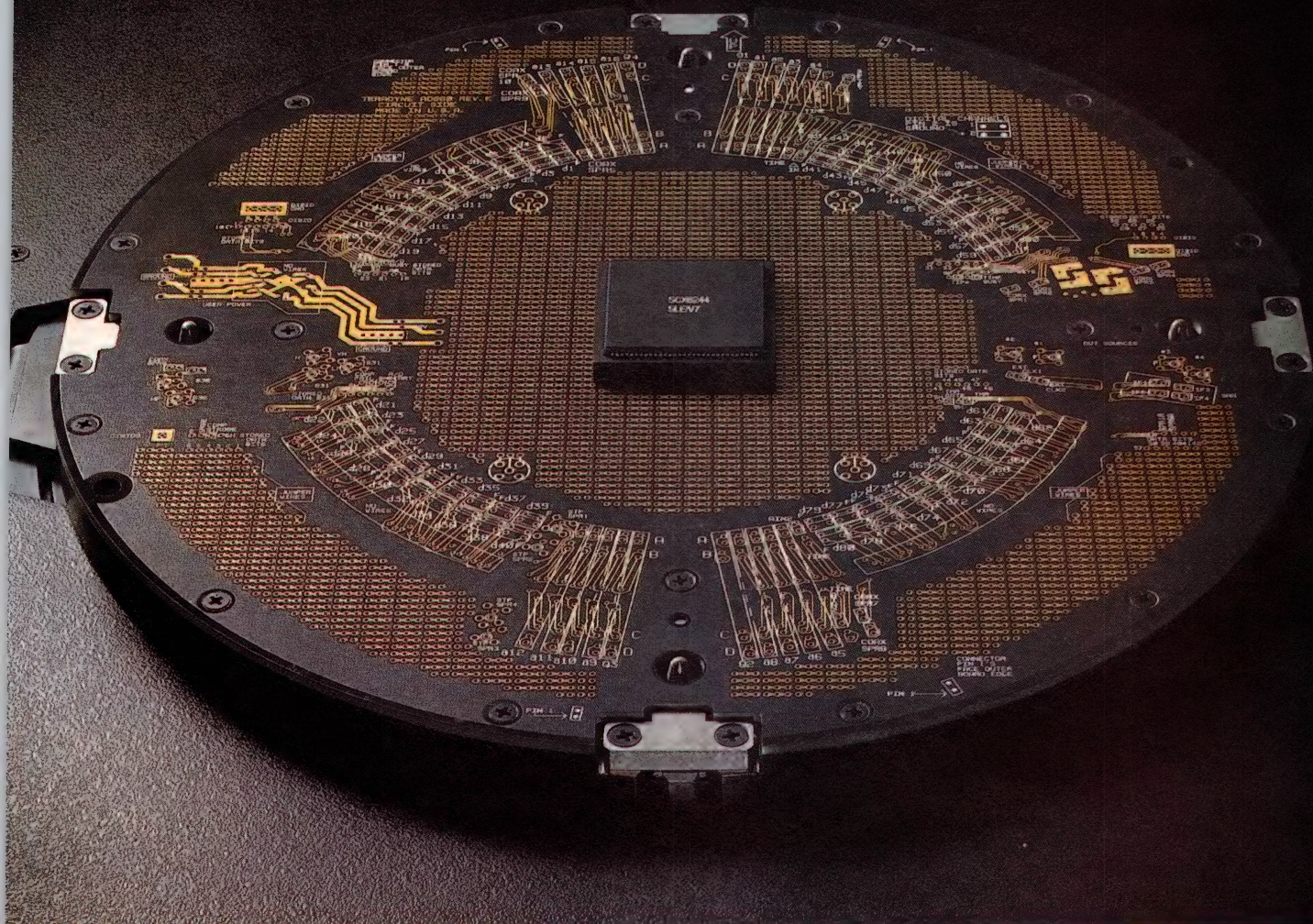
Now there's a family of test systems that will change the way you think about Analog VLSI testing.

The system on the left thinks up new device designs so fast that most test systems can't keep up with it. Except the one on the right.



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Now, you can test anything from standard linear to mixed-signal AVLSI. Teradyne has taken its revolutionary A500 architecture and created two new, compatible systems. The A510, a workstation-based standard linear tester, with the lowest cost



this system can test.

to test per test head, and the A520, which packs all the performance of an A500 into a smaller footprint at a lower capital cost. Teradyne's new A500 family not only gives you the capability to test the range of today's devices, it's ready to help you test tomorrow's devices, as well.

The A500 family shares an architecture based on today's "open systems" standards—dual Sun computers, a UNIX operating system, powerful C-based IMAGE™ software and Ethernet TCP/IP networking. In addition, each system provides full tester simulation on stand-alone workstations, with graphic debug and analyzer tools as powerful as any CAD/CAE tools.

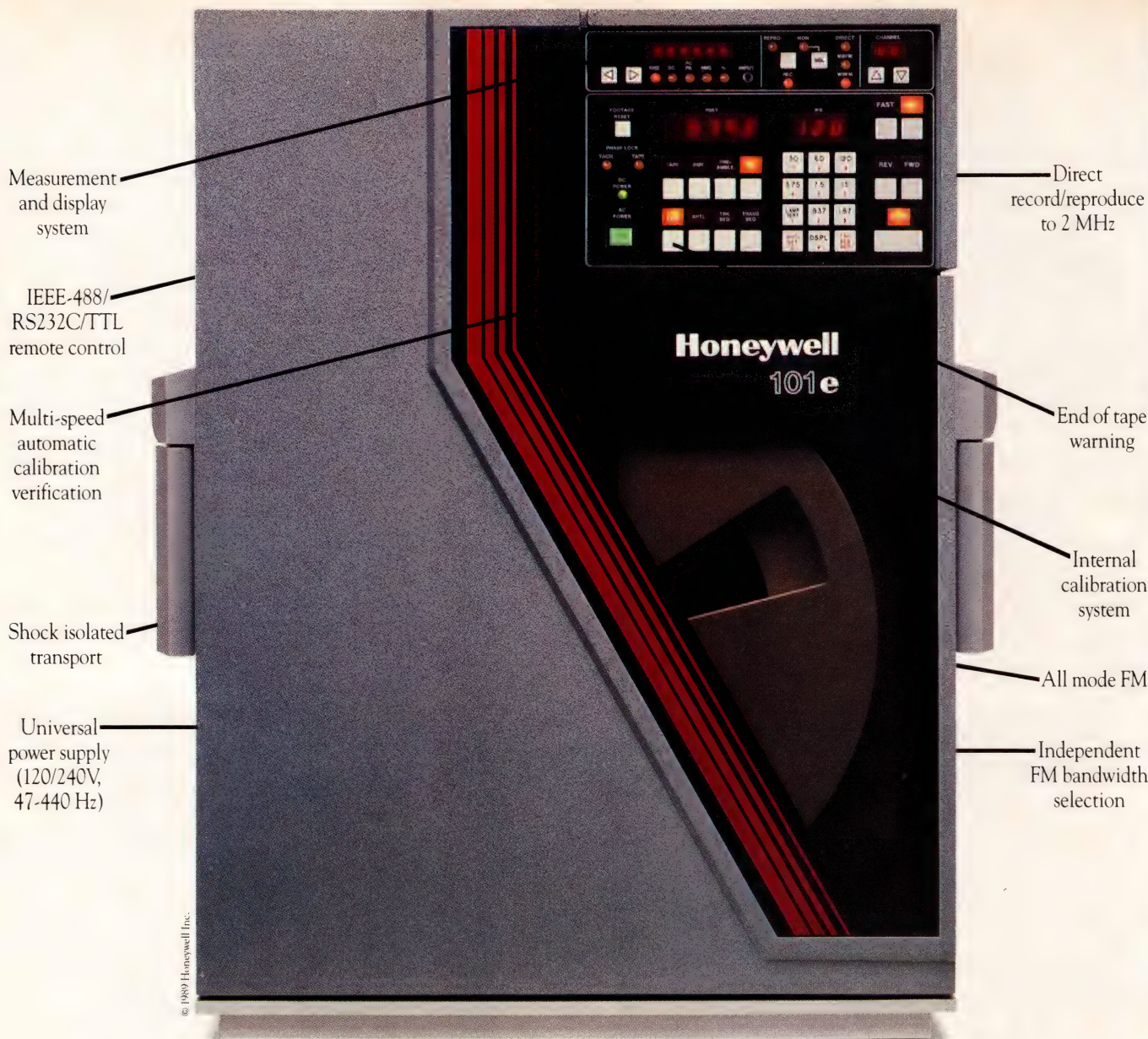
Spend your time testing designs instead of designing tests.

If you want to help your company bring next-generation products to market faster, prevent premature product rollouts and cut test engineering costs drastically, use the system on the left. Which can only lead you to the system on the right.

For more thoughtful details, call Beth Sulak at (617) 482-2700, ext. 2746. Or call your nearest Teradyne sales office or write: Teradyne, Inc., 321 Harrison Avenue, Boston, Massachusetts 02118.

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For details, contact Darrell Petersen, Honeywell Inc., Test Instruments Division, Box 5227, Denver, CO 80217-5227. (303) 773-4835.

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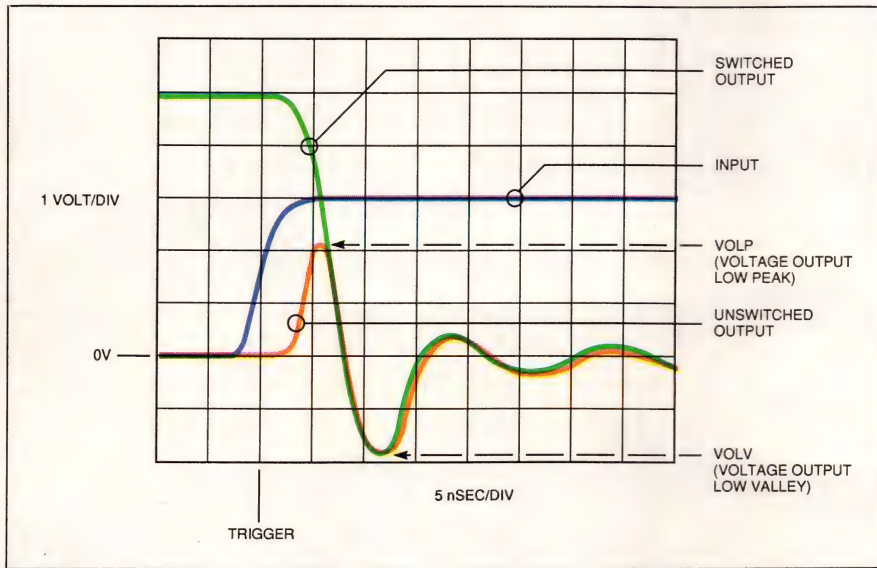
CIRCLE NO 49

SIGNALS & NOISE

A helpful addition

Several readers complained that they had difficulty interpreting the scope photos that appeared in David Shear's Special Report,

"EDN's advanced CMOS logic ground-bounce tests" (EDN, March 2, 1989, pg 88). The reason for the difficulty was the omission of the following explanatory figure.



How to order the VIZ WC-412A R-C box

Recently a reader wrote to me asking where he could buy the VIZ WC-412A R-C box, which I mentioned in the troubleshooting analog circuits series (EDN, January 19, 1989, pg 160). Fordham Radio no longer sells it. Instead, to order the \$119 box, call Dennis Roe at Quement (one of the several distributors that will take your order), 1000 S Bascom Ave, San Jose, CA 95128. Phone (408) 998-5355.

If you wish to find a distributor closer to your location, contact Frank Menichello at VIZ, 175 Commerce Dr, Fort Washington, PA 19034. Phone (800) 523-3696.

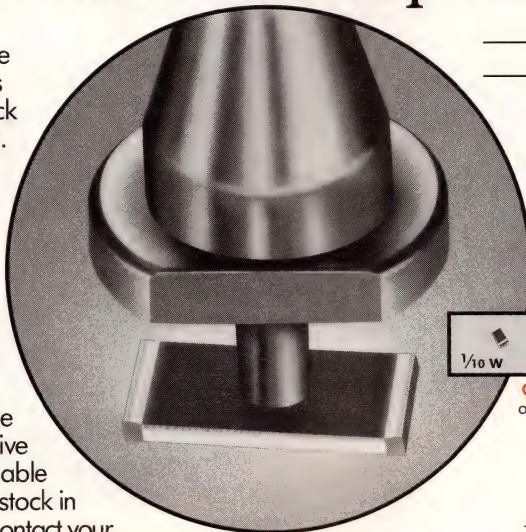
Robert Pease
Staff Scientist
National Semiconductor
Santa Clara, CA

Text continued on pg 40

Pick of the Chips

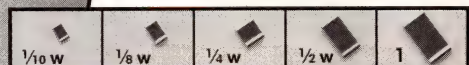
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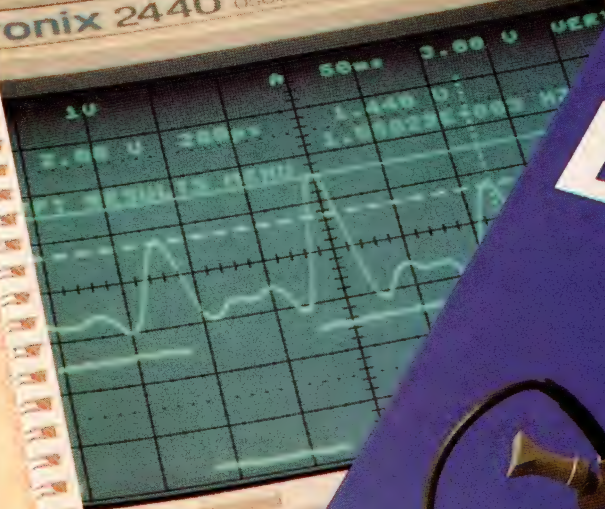
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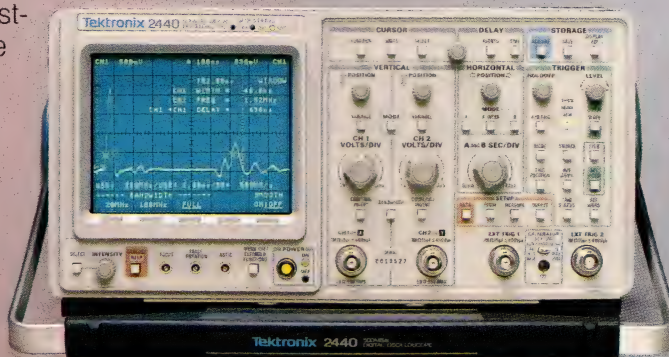
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Thanks for the "great analog stuff"

Thanks very much for publishing the great analog stuff by Jim Williams, Jerald Graeme, and other greats of analog design. The article by Professor Sergio Franco (EDN, June 8, 1989, pg 147) on compensating op-amp circuits with capacitive

loads was a very well-done analysis. I'd like to add for your readers that the analysis assumed an ideal op amp; that is, one with infinite gain-bandwidth product (GBW). For 99% of all current op amps in the world, this analysis is fine, but readers should note that if their circuits have a GBW of <100 kHz, the

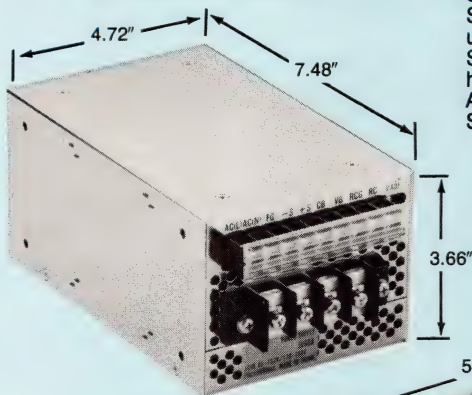
analysis accuracy degrades rapidly, resulting in an undercompensated situation.

This is a very minor point about an otherwise excellent article and analysis. Good work, Sergio!

*Steve Hageman
Chief Engineer
Calex Mfg Co Inc
Pleasant Hill, CA*

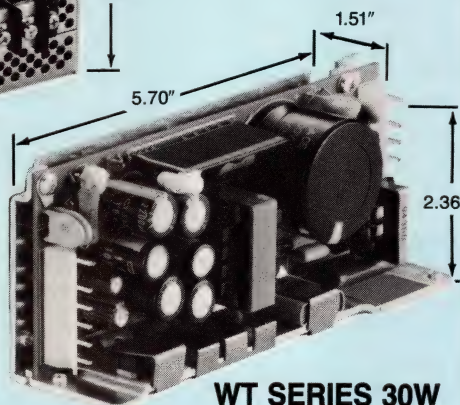
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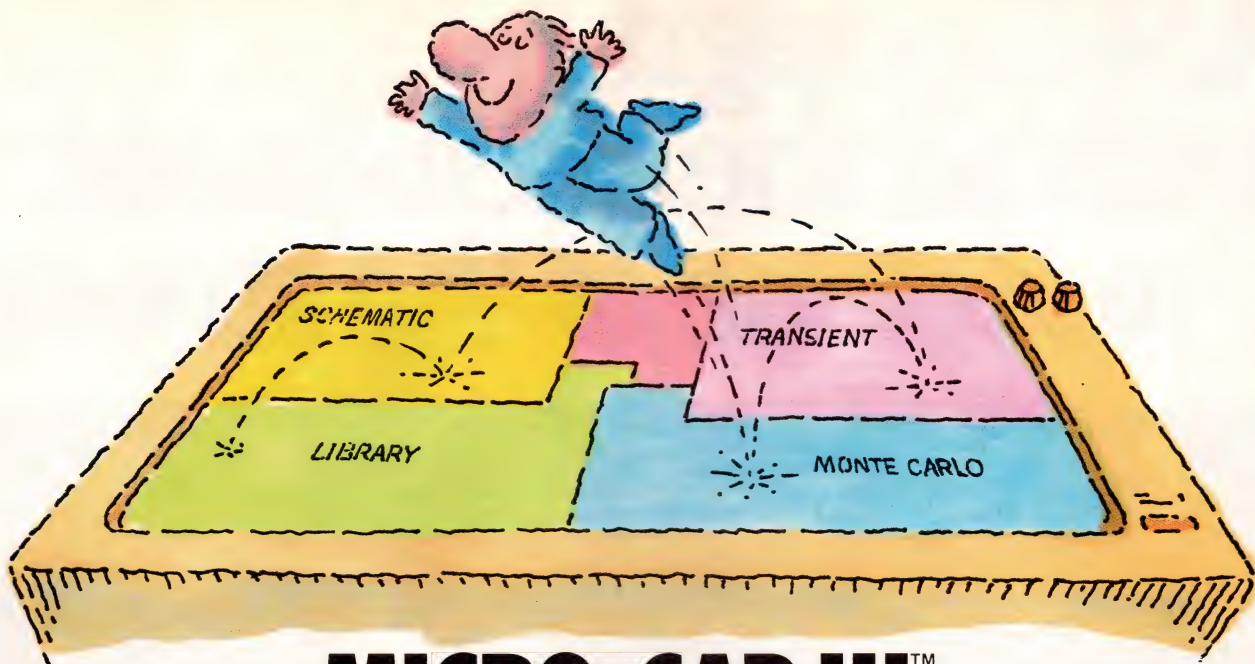
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*Janet Vaniman
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Correction

The article "Circuit design requires thermal expertise" contains an erroneous thermal model on pg 95 in EDN's June 22 issue. This model has been commonly used in the past. If the junction is the source of heat, it must be the hottest point in the 1-D thermal model. The thermal resistances should not be shunted by the thermal capacities that provide a low-impedance transient path. Rather, the capacitances must be connected directly to ground (ambient) from their circuit tie points.

*John P Lintz
Engineering Section Head
Honeywell Inc
Space Systems Group
Glendale, AZ*

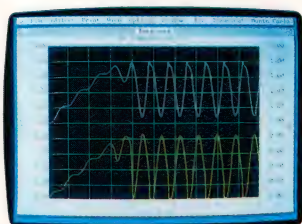


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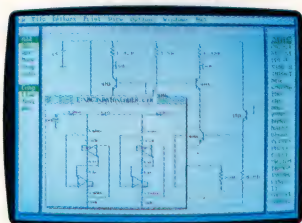
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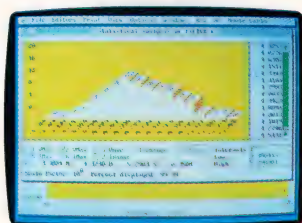
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Buscon '89 East, Marlboro, MA. CMC, 200 Connecticut Ave, Norwalk, CT 06856. (203) 852-0500. FAX 203-838-3710. September 11 to 14.

Midcon/89, Rosemont, IL. Midcon/89, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. September 12 to 14.

Aerospace & Electronics '89 (conference), Santa Clara, CA. National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031. (703) 698-9600. FAX 703-560-2752. September 12 to 15.

SECS Communications Seminar, Boston, MA. GW Associates Inc, 1183 Bordeaux Dr, Suite 27, Sunnyvale, CA 94089. (408) 745-1844. FAX 408-745-6395. September 15.

1989 IEEE Bipolar Circuits and Technology Meeting, Minneapolis, MN. Jan Jopke, Conference Coordination Services, 6611 Countryside Dr, Eden Prairie, MN 55346. (612) 934-5082. September 18 to 19.

IEEE Holm Conference on Electrical Contacts, Chicago, IL. IEEE Holm Conference Registrar, 345 E 47th St, New York, NY 10017. (212) 705-7405. September 18 to 20.

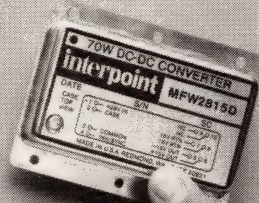
1989 Annual Conference of the International Federation of Consulting Engineers, Washington, DC. Jeanne Quick, American Consulting Engineers Council, 1015 Fifteenth St NW, Washington, DC 20005. (202) 347-7474. September 24 to 27.

Expo SMT International, Las Vegas, NV. Expo SMT, Box 1869, Los Gatos, CA 95031. (408) 354-0700. FAX 408-354-1036. September 25 to 27.

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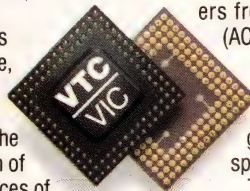
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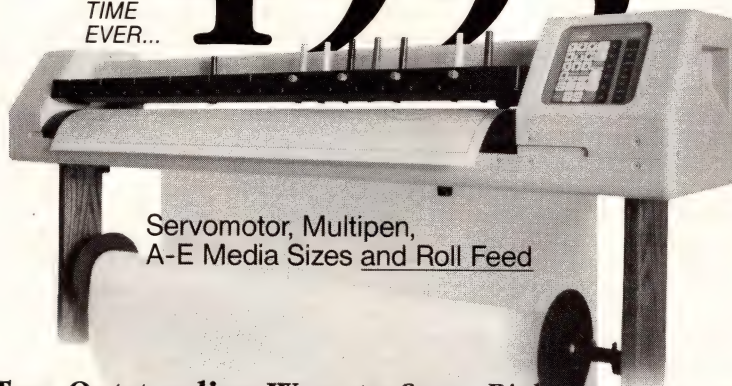
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Diskcon, San Jose, CA. Julie Sunseri, 710 Lakeway, Suite 170, Sunnyvale, CA 94086. (408) 720-9352. FAX 408-736-2523. September 26 to 27.

IEEE International Conference on Computer Design (ICCD '89), Cambridge, MA. Giovanni De Micheli, Center for Integrated Systems, Room 129, Stanford University, Stanford, CA 94305. (415) 725-3632. October 2 to 4.

Electronic Imaging Conference East, Boston MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 2 to 5.

Policy and Parity: The Future of US-Japan High Technology Trade Policy (symposium), Boston, MA. Janet Fannon, Clearpoint Research Corp, 99 South St, Hopkinton, MA 01748. (617) 435-2301. October 12 to 14.

Systems 89, Munich, West Germany. Gerald G Kallman, Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. FAX 201-652-3898. October 16 to 20.

Northcon/89, Portland, OR. Northcon/89, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. October 17 to 19.

Supercomputing World, San Francisco, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 17 to 20.

Unix Expo '89, New York, NY. National Expositions Co, 15 W 39th St, New York, NY 10018. (212) 391-9111. FAX 212-819-0755. November 1 to 3.



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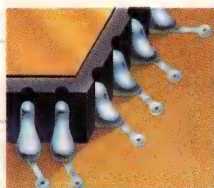
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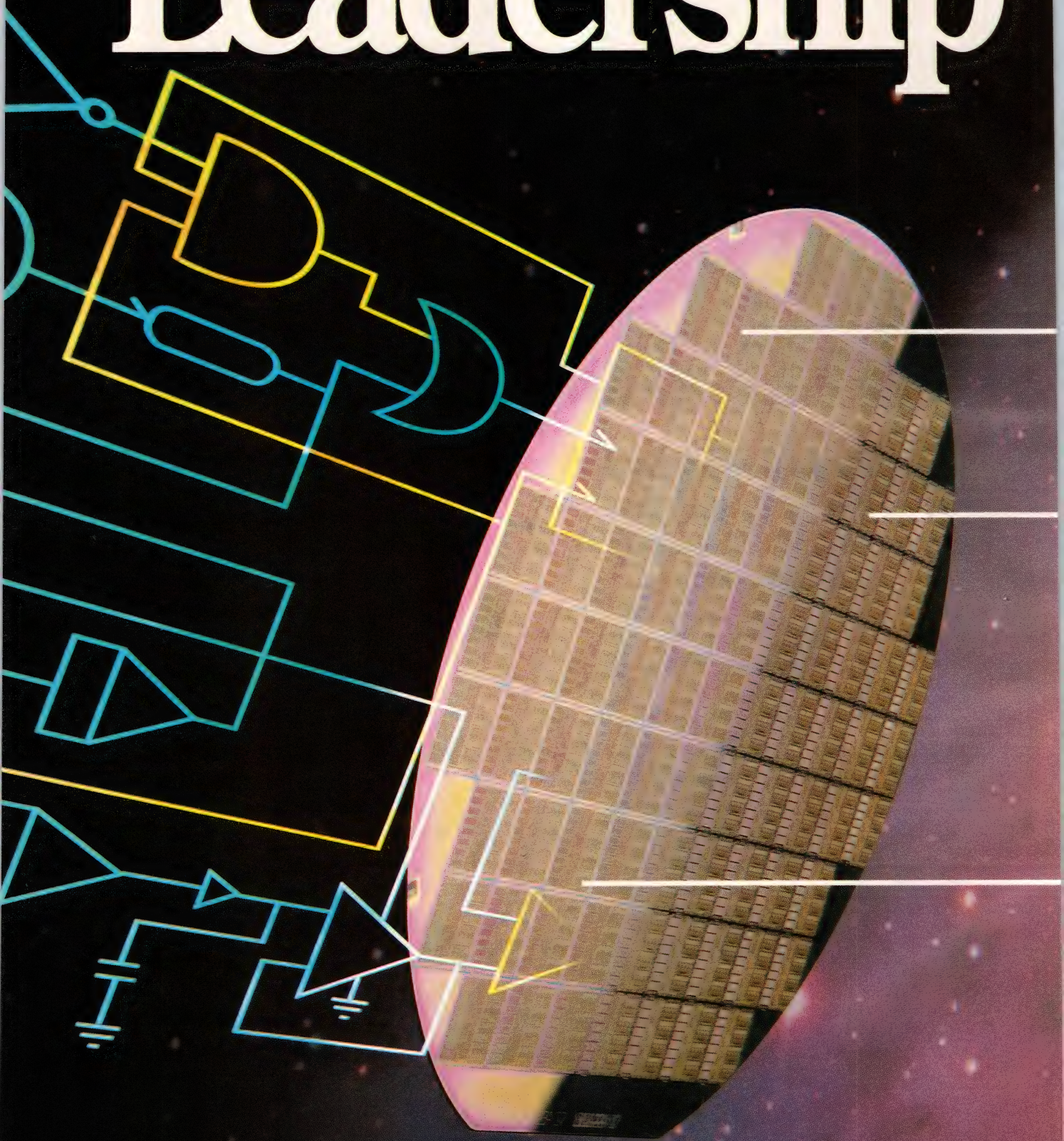
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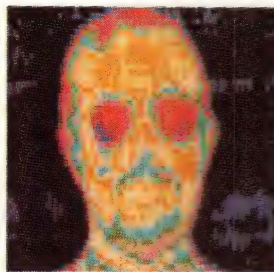
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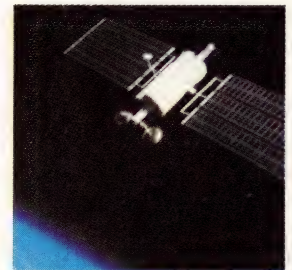
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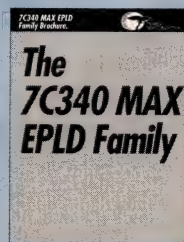
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EDITORIAL

Enjoy life



The summer vacation time has come and gone, and I hope all of you enjoyed some time off during the summer months. Although engineering can be fun, it's important to remember that there is more to life than circuits, computers, projects, and deadlines. All too often we get caught up in our own world of work; we forget to smell the roses, to watch the sunset.

I have a close friend who forgot that life is to be enjoyed. He forgot that every waking hour isn't to be spent taking on more and more work. As I remember being with him, I can recall hardly any time when he wasn't working. Whether he was writing software or toiling in his garden, it was work, work, work. I suppose some of his attitude stemmed from the pressures of the work ethic, but some of it was self-imposed, too.

As a youngster, he was always pushing himself to do more and more, better and better. Never a rest, always moving on to bigger projects. Always trying to achieve more and more. When he went to college, he completed a BS in chemistry and went directly into a PhD program. No time for a rest—he might miss something important. Vacation and time off weren't that important and could be taken later.

Unfortunately, my friend let the work ethic steer him to disaster. After a separation from his wife he moved to a new town to start putting his life back together. But he was still driven by work and even more work. While waiting to start a new job he taught courses at a local community college, took computer courses, and then spent weekends at an Army Reserve unit. He'd take a weekend off some other time. He was also winding up some business affairs and working on two outlines for computer and electronic books he wanted to write. He was pushing himself too hard and trying to do too much, and he wouldn't listen to my advice to slow down.

In June 1985 the pressure caught up with him. Returning from an Army Reserve weekend, he fell asleep at the wheel of his car and hit a tree, sustaining major brain damage. Yes, he wore a seat/shoulder belt and didn't suffer any broken bones. But today, this holder of a PhD works part time in the mail room of a medical facility. He also delivers flowers at a nearby hospital. That's about all he can do. Sometimes he gets disoriented and loses his way. He can't remember which bus to take, so he can't rely on public transportation. He'll never get better and he must live in a supervised housing system. He is 38 years old.

So, the next time you feel the pressure building and think you can't escape from a deadline, remember that the world isn't made up of work alone. Part of life is stopping long enough to enjoy it and to remember how precious it is. We never know how much life we've been given. Don't waste what you've got left.

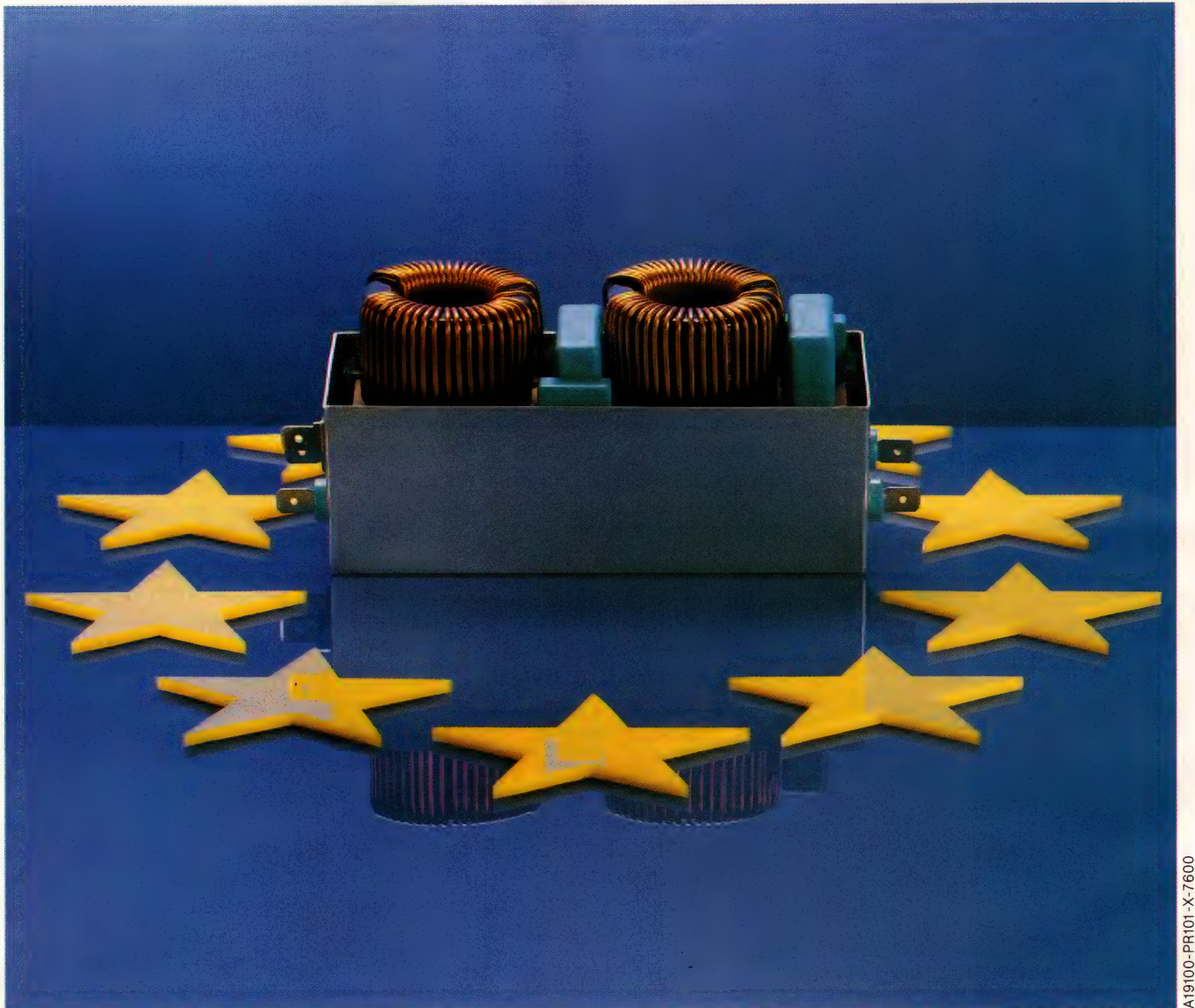


Jesse H. Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
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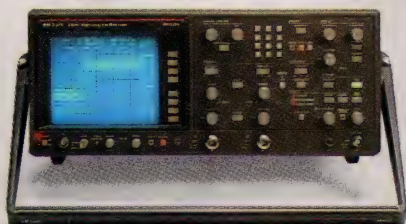


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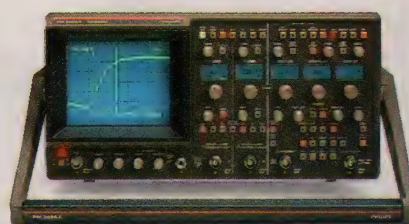
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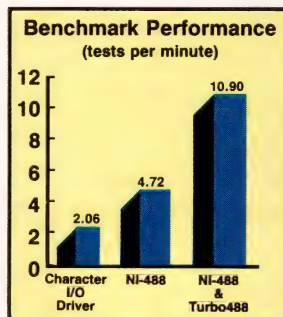
By moving time consuming software functions into hardware, the Turbo488 significantly reduces the overhead of a software driver too. The combination of the AT-GPIB and our streamlined software driver gives you the power needed for today's high speed digitizers.

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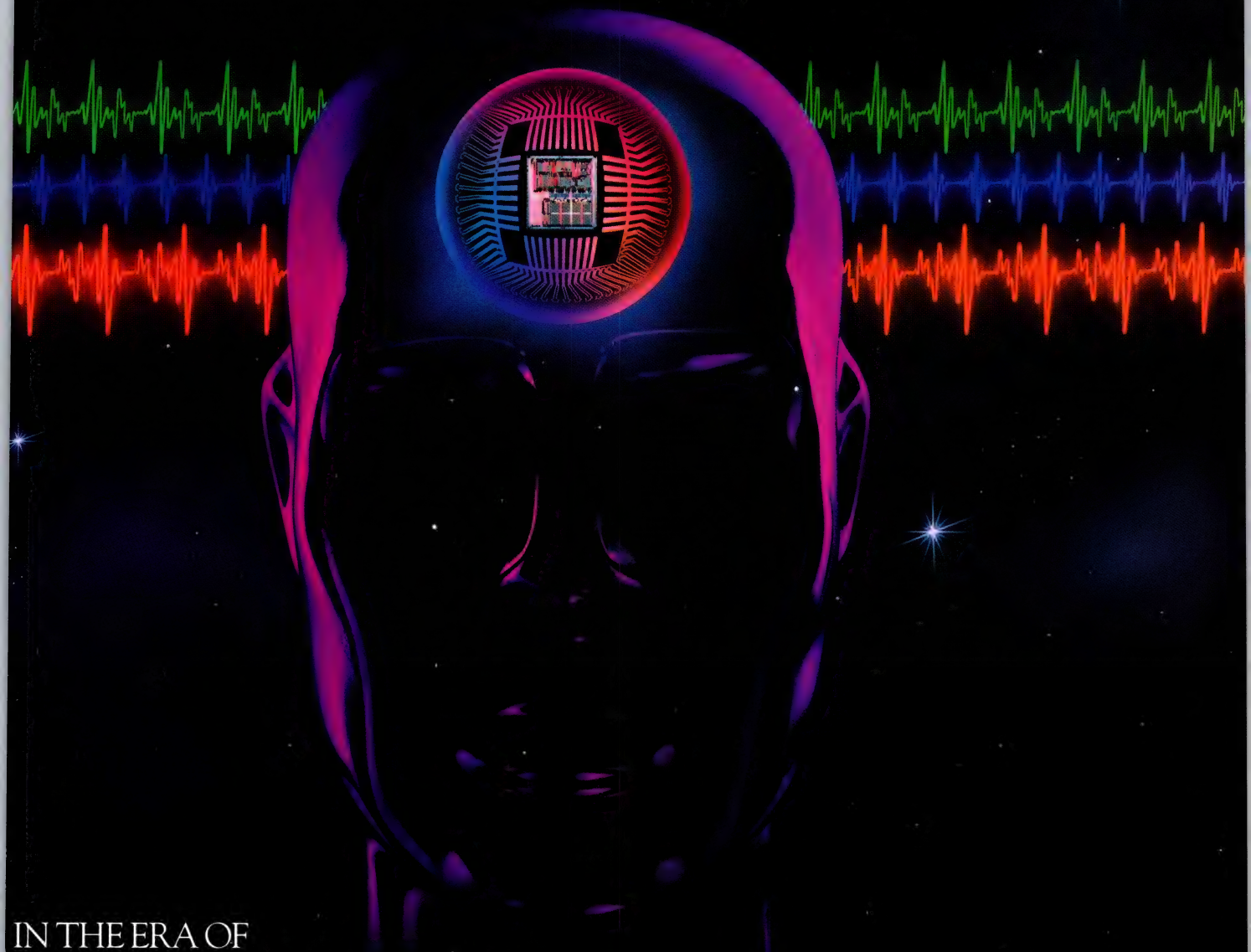
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TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

New ways to link digital brains to advanced analog worlds



IN THE ERA OF

MegaChip

TECHNOLOGIES



Next-generation analog: Advanced Linear ICs

A new breed of linear chips, born of leadership processing at Texas Instruments, can help you design superperformance systems.



The human brain has separate but dependent left and right sides. Similarly, an electronic "brain" or system has separate but dependent parts, one digital, one analog. Designers accustomed to the spectacular performance gains made in digital chips are now demanding comparable improvements in analog devices so that both parts of their systems can function to full potential. Leading the analog evolution: Advanced Linear circuits from Texas Instruments.

These new chips are called *advanced* for one or more reasons. They are more highly integrated than ever before, often combining digital and analog functions on a single chip. They offer higher performance and greater flexibility.

Sophisticated design and simulation tools shorten development cycles of TI's Advanced Linear ICs, helping you get to market faster. By using these tools, TI can offer as standard circuits many designs that previously would have had to have been customized.

They are often the result of advanced processing that may merge two or more technologies.

Better parameters from better processing

Because advanced analog system requirements for performance and flexibility vary greatly, a single workhorse technology typically can't do the job any longer. Nor can creative circuit designs alone. We at TI are convinced the key to driving the linear evolution lies in the excellence of our processing technologies.

TI is committed to developing and implementing a range of leadership wafer-fabrication processes (see *descriptions on back page*). The

result: TI's Advanced Linear devices are already helping system designers link digital brains to advanced analog worlds more efficiently and with greater ease in many applications. Here are a few examples.

Advanced Linear: Displaying greater brilliance

Out of our pacesetting LinEPIC™ processing comes our high-performance Color Video Palette, operating at 125 MHz with a very high-resolution 1024 x 1024 pixel count. Because of one-micron CMOS processing, power consumption is reduced more than 40% compared to other CMOS implementations. Additionally, the device is pack-

...the key to driving the linear evolution lies in the excellence of processing technologies.

aged in reliable, economical plastic.

LinEPIC has also produced such high-speed, high-density interface chips as our Flash A/D and our Video DAC for use in graphics displays, imaging systems, monitors,

chips are ideal for use in automotive antilock braking systems, electronic transmissions, and active suspension systems.

Either technology can produce devices with low-side drive, high-side

to design with—it is available in our LinASIC™ cell library for integration with digital ASICs.

A new family of Analog Interface Circuits (AICs) is emerging from our Advanced LinCMOS™ processing. The voice-band AICs, designed for modems and fax equipment, combine high-performance analog functions—14-bit A/D and D/A converters and switched capacitor filters—with digital functions such as control circuitry, program registers, and DSP interface. The usual clutter of resistors, capacitors, and pots is eliminated.

High-speed AICs are available for use in servo controllers and hard-disk-drive applications.

These AICs are also high-performance members of our LinASIC standard-cell library. Based on TI's proven digital ASIC methodologies, the LinASIC library has allowed us to develop complex, semicustom chips in as little as 16 weeks.

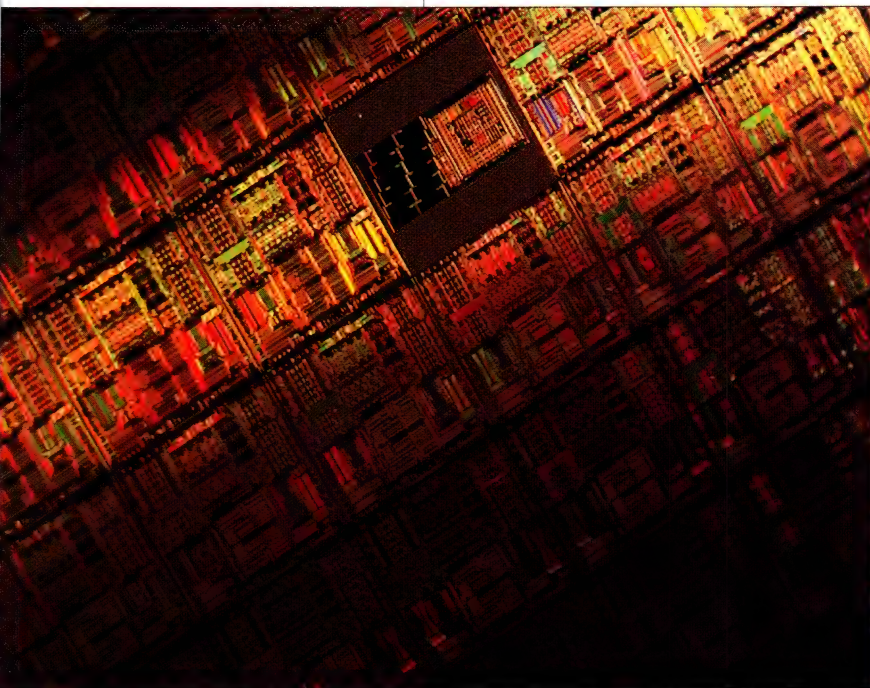
Advanced Linear: Boosting instrumentation accuracy

Even one of the most basic analog building blocks, the operational amplifier, is benefiting from TI's Advanced Linear technologies. Our Excalibur op amp family combines low power consumption with a 5X speed improvement while retaining low offset voltages. Offset-voltage drift has been cut from 300 μ V to 60 μ V to reduce your calibration, test, and measurement expenses.

For high-accuracy applications, Advanced LinCMOS is making possible Chopper Stabilized Op Amps with chopping frequencies 10 times higher than previously available (10 kHz). Noise levels are the lowest on the market.

The evolution in analog devices has only begun. Dramatic progress lies ahead throughout the 1990s. As the Advanced Linear leader, Texas Instruments is pledged to remain at the forefront, supplying you with new ways to link digital brains to advanced analog worlds.

For suggestions on choosing a linear supplier, turn the page.



High-density Analog Interface Circuit chips demonstrate the greater integration achieved by TI's innovative linear processing technologies. These DSP interfaces allow you to alter circuit configuration under software control without external adjustments.

and cameras. Both devices require about five times less power than bipolar equivalents.

Advanced Linear: Intelligent power for every car

Chips fabricated with our Power DMOS-based BIDFET™ processing are replacing electromechanical relays in many automotive applications, such as driving headlamps and motors. Power BIDFET allows us to minimize power loss in the switch and add high-complexity logic functions.

Multi-EPI bipolar processing, a very cost-effective technology, is used to produce chips having inherent reverse battery protection and high operating voltages. Such

drive, or H-bridge configurations.

In the future, these developments may lead to multiplexed systems for cars, replacing bulky wiring harnesses.

Advanced Linear: Enhancing modems and facsimiles

TI's dual driver/receiver is a good example of the integration achieved with advanced processing technologies. LinBiCMOS™ processing has enabled us to put the drivers and receivers needed for RS-232 voltage levels on the same chip with the charge pump required to generate the necessary split rails from a single 5-V supply. You eliminate external power supplies and get a device that's easier

40% of all CMOS and BiCMOS standard-cell and compiled chip designs will have less than 5% of the chip's transistors used for analog functions.

56% of designs will have 5%-50% analog content.

4% of designs will have more than 50% analog content.

PERVASIVENESS OF ANALOG FUNCTIONS IN ASICs BY 1990

Source: The Technology Research Group, Inc.

Circuits combining analog functions with digital logic will soon be widespread in ASIC chip designs. TI is taking a leadership role with the development of its LinASIC methodology.

Checkpoints for choosing an analog supplier in the 1990s.

Questions and answers with Tom Engibous, Vice President, Semiconductor Group, and Manager, Linear Products, Texas Instruments Incorporated.

Q. What is the first thing to look for in choosing a linear supplier?

A. Product performance is definitely the first priority. Our customers are asking for ever-increasing linear device performance. At TI, we believe creative circuit designs alone won't meet the challenge. Advanced process technologies—note the plural—are becoming the keys to success in linear device performance of the '90s.

Q. What else should a designer look for?

A. Whether or not the supplier has experience with digital as well as analog devices. These two worlds are merging (see chart above). Functions once performed by analog are now done digitally, and a growing percentage of our Advanced Linear devices combines analog and digital circuitry on one chip.

At TI, we've leveraged our 30 years of digital expertise into the development of our Advanced Linear products and processing with highly satisfactory success. This has been especially noticeable with our LinASIC methodology.

Q. Do you expect ASICs to play a major role in your linear future?

A. Very definitely, as they already do today. Cell-based designs will be the rule in both user-specified functions and highly integrated stan-

dard products. Digital ASIC methodologies are also the key to cutting system design cycles. As our digital experience proves, suppliers who have advanced process technologies and fast, accurate design-automation tools will be the best equipped to deliver single-chip solutions.

Today, we have customers doing their own LinASIC designs using our advanced processes and design-automation tools.

Q. What role does manufacturing capability play in picking a supplier?

A. It is always a factor, and the need for efficient worldwide manufacturing facilities such as TI has in place will become even more important. Today's semiconductor market is global in nature. You can't serve worldwide customers from a single plant—you have to be "multilocal." This is particularly true with ASICs.

Q. Any other important factors?

A. Yes, I'd suggest that, in choosing a linear supplier, the designer find one he can live with for a long time. Close supplier-customer relationships are essential to the development of products that will provide the highest performance and lowest cost systems.

TI's Leadership Linear Processing Technologies

LinBiCMOS—Combines Advanced LinCMOS, digital ASIC CMOS, and up to 30-V bipolar technologies to allow the integration of digital and analog standard cells and handcrafted analog components on a monolithic chip.

LinEPIC—One-micron CMOS double-level metal, double-level polysilicon technology which adds highly integrated, high-speed analog to the high-performance digital EPIC process.

Advanced LinCMOS—An N-well, silicon-gate, double-level polysilicon process featuring improved resistor and capacitor structures and having three-micron minimum feature sizes.

Power BIFET—Merges standard linear bipolar, CMOS, and DMOS processes and allows integration of digital control circuitry and high-power outputs on one chip. Primarily used for circuits handling more than 100 V at currents up to 10 A.

Multi-EPI Bipolar—A very cost-effective technology that utilizes multiple epitaxial layers instead of multiple diffusion steps to reduce mask steps by more than 40%. Used to produce intelligent power devices that can handle loads as high as 20 A and voltages in excess of 100 V.

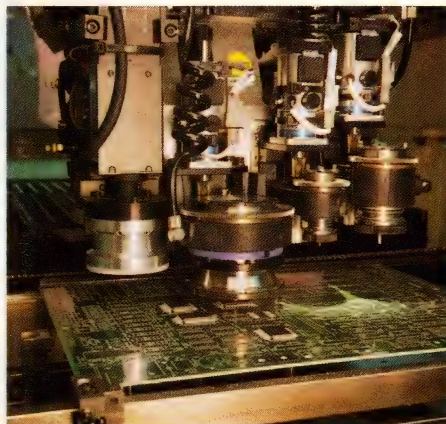
Excalibur—A true, single-level poly, single-level metal, junction-isolated, complementary bipolar process developed for high-speed, high-precision analog circuits providing the most stable op amp performance available today.

Our just-published *Advanced Linear Circuits* brochure examines more fully the changes taking place in analog system design and their impact on linear devices. The brochure also describes TI's leadership processing technologies and explains the performance improvements that result. **For your copy, call 1-800-232-3200, ext. 3407, today.**

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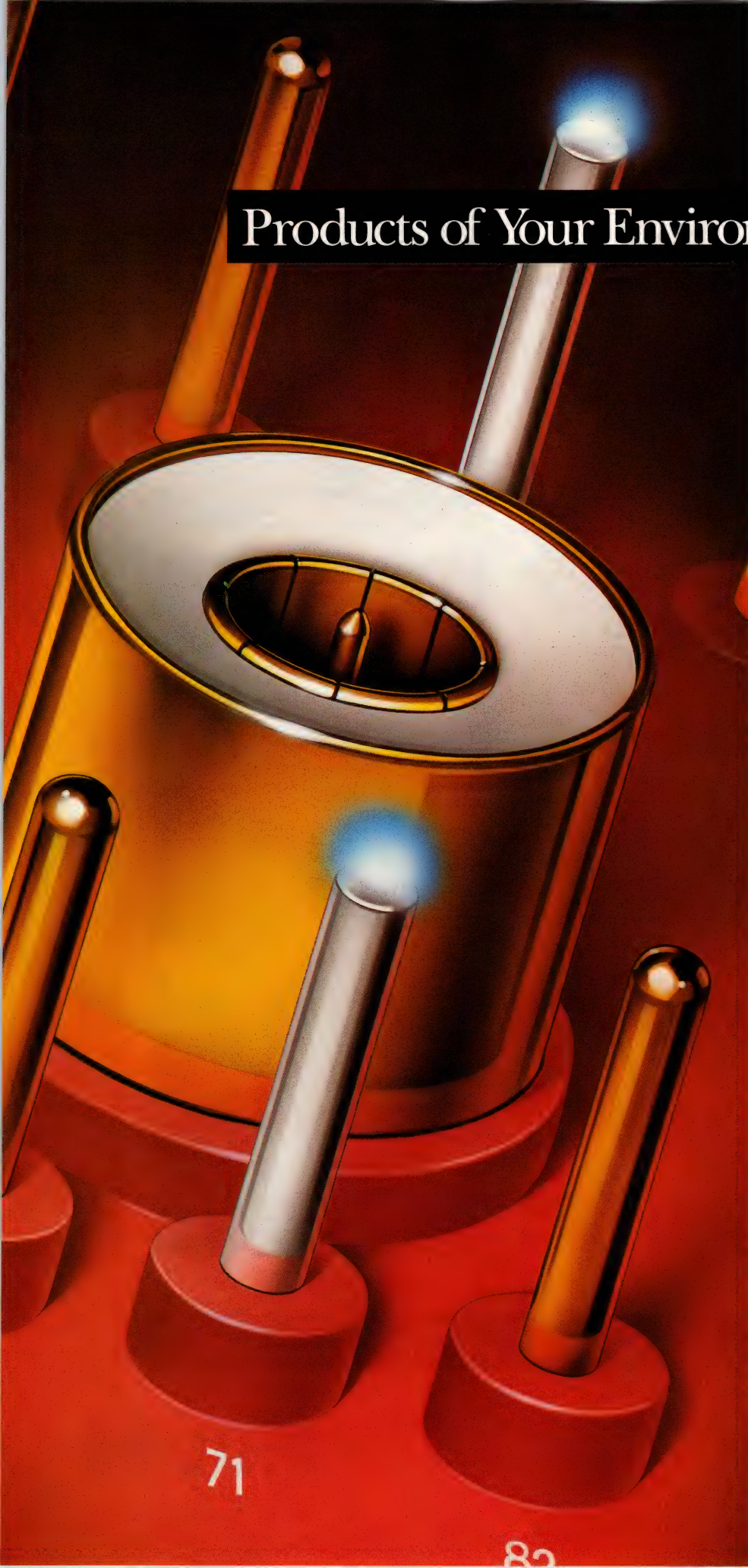
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CIRCLE NO 58

Hardware and software keep your PC data safe



PC operating systems have no built-in security safeguards. To keep your data safe, you must deny snoopers access to the computer, encrypt your files, and lock up your primary storage at night.

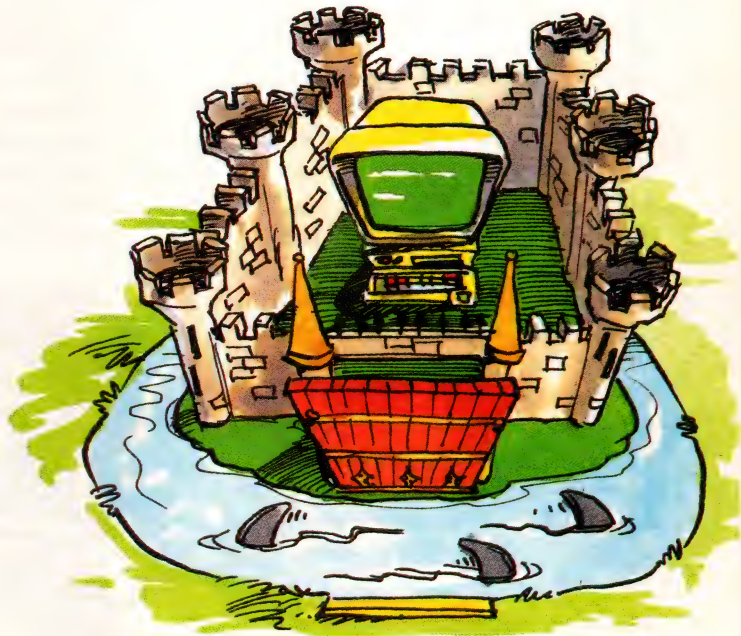
Chris Terry,
Associate Editor

As PCs and workstations become standard office tools, their users must be as cognizant of computer security as users of the erstwhile dominant mainframes. Office PCs and workstations are liable to store, or have access to, files that contain sensitive data that was once found only in the mainframes of an MIS department: personnel files, current financial operations and projections, and proprietary or classified design and manufacturing data (particularly in companies that handle DoD contracts).

The question then arises: How much security is enough? Companies that handle DoD contracts have no choice—NSA-approved security equipment and procedures are mandatory. But even companies that don't handle classified information must protect the data on which their business depends, and they must strike a balance between doing nothing (which leaves them open to disaster) or installing such stringent security measures that productivity suffers (which may result in users trying to ignore these measures, or merely being sloppy about observing them).

The security problem is further compounded by the increasing use of computer-to-computer communications over

local-area networks, as well as over the PSTN (Public Switched Telephone Network). There are key issues you must consider if your company has reached the stage where some security measures have become essential. These measures fall into three general categories:



Illustrations by Jon McIntosh

- Denial of unauthorized external access to a running computer (computer phreaks, worms, viruses)
- Denial of unauthorized internal access to individual files in a running computer (accidental or deliberate snooping by an employee)
- Protection of active and archived files associated with an unattended or shut-down computer.

Most security experts agree that the best protection against snooping is to

TECHNOLOGY UPDATE

Computer security

deny all unauthorized persons any access to the computer; however, any computer system that allows operation by a remote user via a modem and telephone line is to some degree vulnerable. There are several possible ways to make an external user prove that he is who he says he is. If you're concerned about unauthorized modem access, a call-back security device will probably meet your requirements. A call-back device denies all access when the external applicant first establishes a connection. Instead, the device prompts him for a password and immediately hangs up. The communications software looks in the password file (which may itself be encrypted for extra security) to find the password supplied by the applicant and, if successful, it returns the telephone number associated with that password; the call-back device then dials that number, establishes a modem connection, and permits the applicant to go through standard log-in procedures.

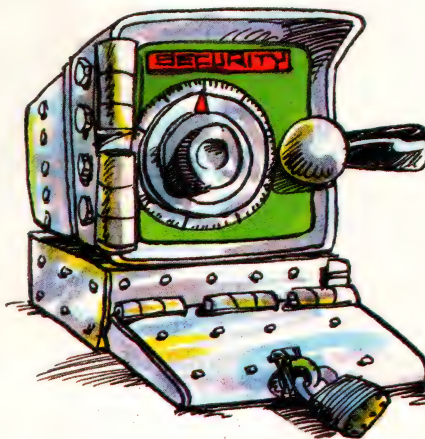
One such device, the 232MSD Modem Security Device from B&B Electronics (\$129.95), handles a single communications port and works with most stand-alone modems that are compatible with the Hayes AT command set. There are also more expensive multiport security devices for use at mainframe or mini-computer sites. Call-back security devices are highly effective barriers to unauthorized modem access—even if a snooper steals or discovers a valid password, it won't get him even as far as the log-in procedures, because he won't be at the genuine user's phone number.

Typing style can identify you

A hardware/software package that verifies one or more physical characteristics of the applicant is another effective guarantee that a local or remote applicant is indeed

an authorized user. You can obtain peripheral devices that verify the applicant's handwriting, voiceprint, fingerprint, or retinal image. Usually, only large installations that handle highly classified information can justify the high cost of these peripherals and the heavy software overhead.

Electronic Signature Lock Corp offers its ESL software package (\$500 for a single PC to \$100,000 for a customized mainframe version) for single-user or networked PC installations. This package analyzes the applicant's keystroke patterns while he enters a password or other set phrase. The software constructs a relative timing profile based on the intervals between the characters and compares this profile to the reference profile that was stored when the applicant was first authorized. Of course, each person's typing, like a signature, shows variations induced by the moment-to-



moment circumstances, state of health, and so on. However, the program uses very sophisticated statistical algorithms that take into account such variations. The company claims that the probability of an unauthorized person gaining access is less than one in one million, even when that person knows the access phrase or password. For high-security installations, it offers

a more elaborate package, CESL, which continuously monitors the user's typing patterns and can detect whether the current user is the same one who was originally given access. The CESL can even determine if the user is under abnormal stress.

Permission-level hierarchies

Mainframe operating systems nearly always have a multilevel access-control system that grants you permission to read, write, or execute your own files, but restricts your access to other files according to the authorizations granted by the system administrator or by the files' owners. Some LAN file servers implement a similar multilevel system. In addition, individual application programs (such as database managers) may add their own system of read/write permissions.

If everyone strictly observes all the rules and frequently changes passwords, the passwords and multilevel permission layers give adequate protection against casual snooping or accidental access to protected files. But there are several loopholes that should be plugged. First, individual users often choose insecure passwords (four to six characters, often a birthdate, license plate number, or some similar personal parameter that is easy to remember). Such passwords are much too short to offer any real protection against guesswork by a determined snooper who has some knowledge of the company and its computer users.

Further, a knowledgeable and determined snooper who has gained permission to log on may then be able to access (and even modify) the file containing the passwords themselves. Although a mainframe OS may have additional safeguards against this, PC operating systems such as MS-DOS and OS/2 have no

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such built-in safeguards and no privilege levels—once you have gained access to the operating system you can do anything that an authorized user can do, such as reading, changing, or deleting data files or formatting the disk to destroy all data.

A software package that erects effective barriers against unauthorized access to the files stored in a shared PC is Fischer's Watchdog (\$295). On IBM PCs or compatibles, software-protection packages are usually installed on the hard disk and are automatically invoked when you boot (or reboot) the system from one of the logical drives on the hard disk (usually the C: drive). You can (unintentionally or deliberately) defeat such packages by booting from a floppy disk, using a system disk that doesn't call up the protection package. Watchdog forces you to boot from the predetermined drive, prompts you for your password, and then places you in a shell that displays only the directory areas for which you are authorized. The system administrator can set the permission levels for the system, for each directory area, and for each user. He can also designate certain directory areas as "secure;" files in secure areas are automatically encrypted, using the company's proprietary encryption algorithm.

Furthermore, Watchdog can deny such dangerous commands as **FORMAT** to all except the most privileged user. As an additional security aid to the system administrator, Watchdog provides an automatic audit trail of all system activities, by user, and reports any attempt to violate permission levels.

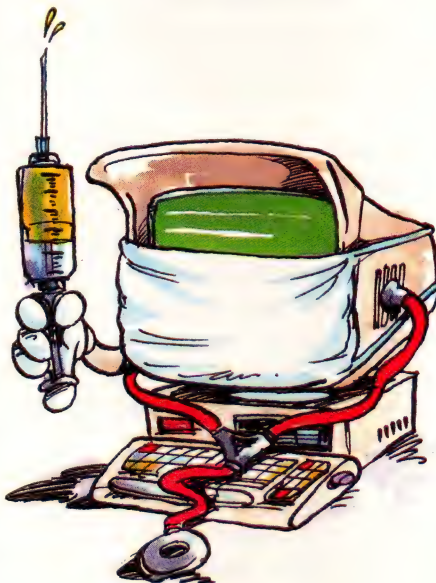
An additional safeguard from Fischer is **Armor** (\$150), a half-card that absolutely defeats an attempt to boot from any drive except the predetermined one, making it im-

possible to bypass Watchdog. The half-card also provides hardware Data Encryption Standard (DES) encryption/decryption of secure files, which is considerably faster than the software algorithm.

Malice aforethought

From wormses and horses,
And dativorous beasties,
And disks that go bump in the
night,
Good Lord, deliver us.

—A Programmer's Prayer



Users and operators of public bulletin boards have for some years been aware of the existence of various kinds of destructive programs. The three main categories of destructive programs are the worm, the Trojan Horse, and the virus. All of them enter your system unbeknownst to you via a seemingly innocent floppy disk or via some loophole in your security measures. A worm attaches itself to an executable program (often **COMMAND.COM**) and forces your system to replicate the worm and run it. A worm doesn't usually do much harm to your data files, but creates a state in which worms call and run

other copies of the worm until all your computer resources are tied up. The most famous (or infamous) example is the worm that immobilized nearly 7000 Unix systems on the Internet network in November 1988.

A Trojan Horse appears to do something useful, but also does something destructive, such as deleting or mutilating files. Trojan Horses don't usually replicate themselves, but can be made to look like a valid command, so that the damage increases every time you run that command.

A virus not only does some damage, but can also infect other executable programs, so that every time you run one of the infected programs, the damage (and the degree of infection) increases. Further, if an infected program can move from one machine to another (as it might do over a LAN), it can infect all the programs resident in the target machine. You may not know, until it's too late, that your system is infected; many known viruses lie dormant until a trigger (such as a date or other random or periodic key) sets off both self-replication and the damaging action (such as deleting files or reformatting your hard disk).

Viruses are becoming more of a problem, and all you can do is install a virus detector, a virus remover, or both, and be alert for signs of unusual activity. And never, never run a new program (especially one residing on a diskette from an unknown source) until you've thoroughly checked it with antiviral tools.

There are two types of virus detectors: integrity checkers and monitors. Integrity checkers let you create a unique checksum or other signature for each program on your disk, and at bootup time examine each program to see if the signature

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has changed. If so, they alert you to a possible problem. Some integrity checkers, such as MDC Software's \$59.95 Integrity Shell, check the signature each time you run a load-and-execute instruction; if the signature doesn't agree with the reference signature, execution is inhibited. Integrity Shell uses a pseudo-cryptographic checksum that is more difficult for viruses to break than the more usual cyclic redundancy checksum (CRC). Monitors continuously examine the interrupt activity and alert you if something occurs that the program's author thought was suspicious.

Virus removers examine all the files on your disk and attempt to find the footprints of viruses known to the authors of the remover. The best programs automatically remove known viruses; at the very least, the program will alert you to a possible problem. The best-known virus removers are WorldWide Data Corp's \$129.95 Vaccine and Computer Integrity Corp's \$69.95 Vaccinate Plus, but there are many others for IBM PCs and compatibles, Macintoshes, and Unix systems.

Remember, virus removers can't detect viruses that are not known to the authors of the remover. When evaluating an antiviral program, your best policy is to check how many viruses the program will handle or how many updates there have been—and don't forget that your backups, as well as your hard-disk-resident programs, may become infected. Check, check, and recheck!

Encryption—the final bastion

If you're seriously planning to protect your sensitive data files, the best way to do so is to encrypt them. Some people are less than enthusiastic about encryption, argu-



The Plus Passport removable hard-disk drive comes with an external or internal base housing, a 20M- or 40M-byte drive that slides out of the housing by releasing a catch, and a PC or Micro Channel adapter.

ing that a determined data thief can often decrypt your files. But, if you use one of the programs that implement the NSA-approved DES algorithms in hardware or software, the data thief had better also be a damned good cryptanalyst (or else have somehow persuaded you to disclose the decryption key for each file).

Encryption is particularly necessary when two or more nodes of a LAN must share sensitive files. A large LAN is likely to have a network analyzer attached to it for troubleshooting and corrective maintenance. The danger is that a network analyzer can not only intercept and display all traffic passing over the network but can also, in the hands of a knowledgeable snooper, be made to simulate a node that has authorized access to sensitive data.

Fischer's Armor half-card implements the DES algorithms in hardware and works very quickly. This card automatically encrypts and decrypts files that reside in directories designated as "secure" by the Watchdog program.

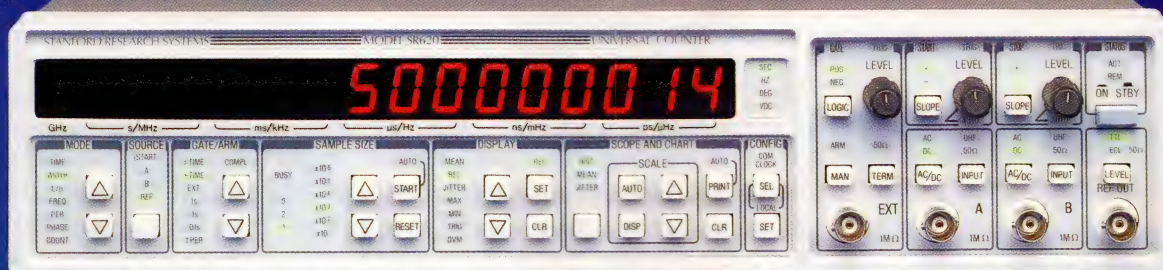
There's a raft of Terminate-and-Stay-Resident (TSR) or stand-alone

programs that implement the DES algorithms in assembly language; these are slower than any hardware implementation, but they're fast enough for day-to-day use. Two of the least expensive are Borland International's \$69.95 Superkey and Wisdom Software's \$69.95 File Encrypt.

Superkey includes DES encryption/decryption among a host of other features, such as keyboard redefinitions and macros, data-entry format control, command-stack editing and recall, single-key screen blanking, and keyboard locking. Fast screen-blanking is valuable if a visitor approaches while you're displaying sensitive data; the keyboard lock is handy if you have to leave the room while you're in the middle of a job. The keyboard-lock feature disables the keyboard (and doesn't allow even Ctrl-Alt-Del re-booting) until you enter your password.

If you're really in a hurry to get a file encrypted, Superkey lets you use Borland's proprietary encryption algorithm which, though less secure than the DES algorithm, is much faster. To highlight the difference, Borland's support department

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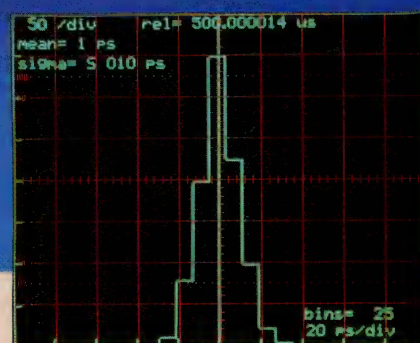
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ran a speed check of both methods. The original file was a 496k-byte text file. Using the DES method, encryption took 4 minutes and 8 sec (2k bytes/sec); the proprietary algorithm completed the encryption of the same file in 42 sec (11.8k bytes/sec). Thus, the proprietary algorithm is nearly six times as fast as the DES algorithm. Both methods write the encrypted version over the original clear-text version.

File Encrypt runs either under MS-DOS or OS/2, and creates a separate file in which it places the encrypted version; the clear-text version remains in existence under the original filename. Although cryptologists generally consider allowing clear and encrypted versions of a file to exist *anywhere* simultaneously to be extremely bad practice, there are two good reasons for this apparent breach of security. First, one of the requirements of the DES is that it should be impossible to reconstruct the encryption/decryption key, even if the cryptanalyst has both the clear and

the encrypted versions to work on. Thus, the temporary presence of both versions is unlikely to have any serious consequences.

Second, Wisdom Software considers it much more important to guard against a power failure or machine malfunction that might leave the file in a partially encrypted state—in the case of a binary file it would then be impossible to determine where encryption ended in order to reconstruct the file. For this reason, File Encrypt leaves the original file intact. However, after successfully encrypting a file, you should immediately make use of the program's option to overwrite the original clear-text file with zeros before deleting it, so as to make it impossible to recover the clear text except by decrypting the file.

At 1.3k bytes/sec, File Encrypt is slower than Superkey, but if you're a consistent victim of Murphy's Law you may be inclined to give more weight to File Encrypt's data-integrity precaution.

One other problem needs to be considered when you plan to safeguard your data: What happens to security when you shut down the computer and leave the building? If you're lucky, your computer is in a room that is kept locked after hours; if you're sensible, you've installed some of the protective measures that were discussed above. But locks are not thief-proof, cleaners have to sweep up (though possibly under supervision), and a really determined snooper with enough time and ingenuity might be able to gain access to sensitive data stored on your hard disk.

NSA has taken the bull by the horns by bluntly declaring that all disk drives and other media containing classified data must be removed and locked in a safe when the computer is unattended. Even if you don't handle classified data, you might want to consider this somewhat drastic procedure, at least for your most sensitive and valuable files.

There are several ways to

For more information . . .

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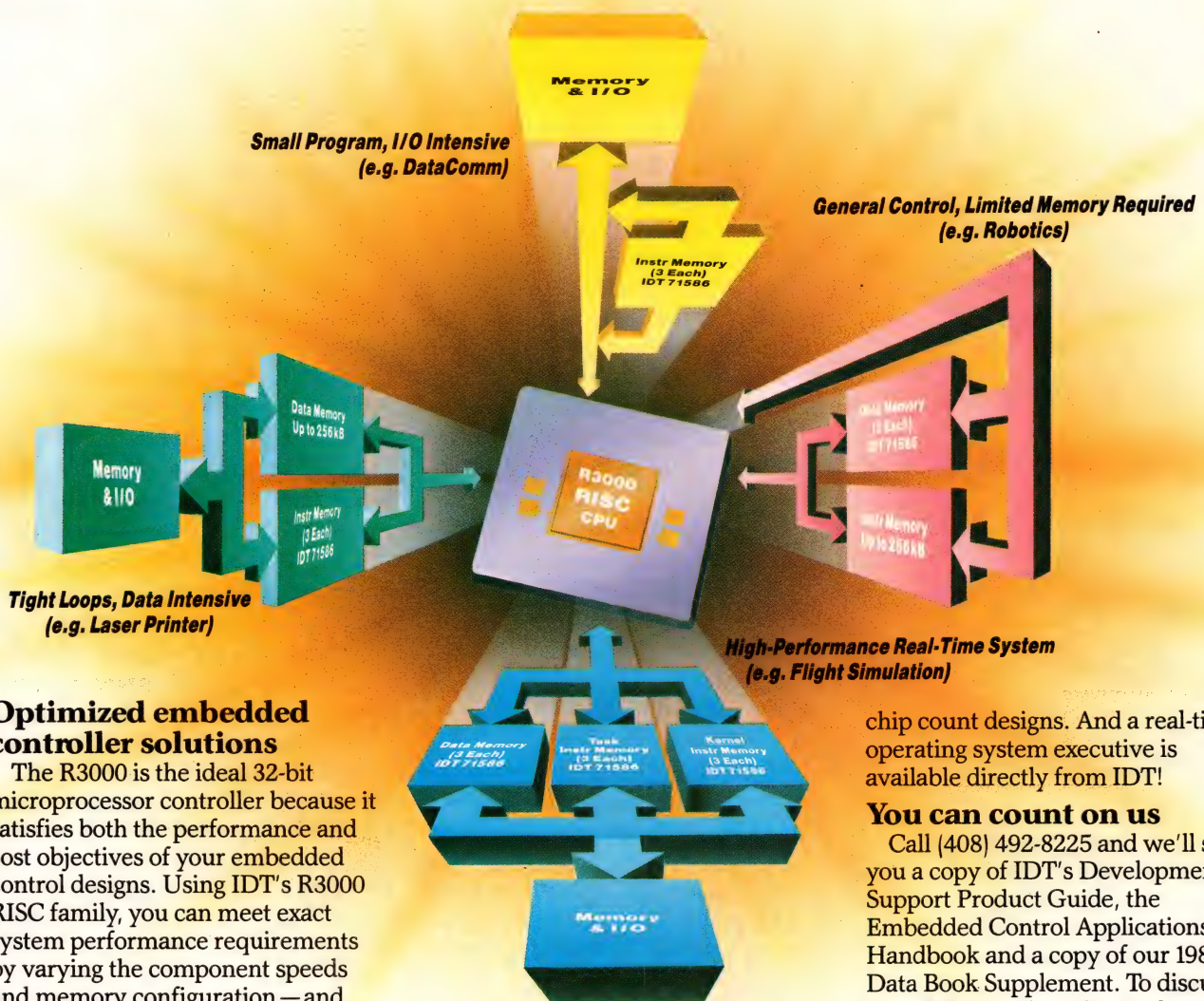
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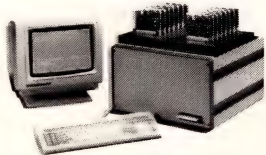
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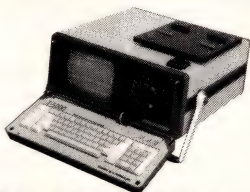
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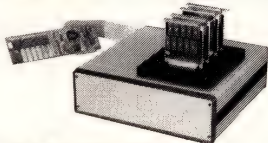
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achieve removability of your primary storage devices. You can use an external hard-disk drive with its own power supply; such a setup requires extra space and may not be easy to disconnect and reconnect daily because it's primarily designed for permanent installation. You can also use a Bernoulli Box from Iomega, which provides removable cartridges. You can get single drives for internal mounting in a PC; external units come with one or two 20M- or 40M-byte drives and a power supply. Prices start at \$1100 for a 20M-byte internal drive. The Bernoulli Box does not use Winchester technology and is somewhat slower than other hard disks, but it may meet your requirements. The media cartridges are certainly easy to handle and take up very little space.

Plus Development's Plus Passport removable drives may suit you even better, because they are internal drives that are specifically designed for frequent removal and replacement. They consist of two parts: a base housing and PC or Micro Channel adapter (\$650); and a 20M-byte (\$595) or 40M-byte (\$795) hard-disk drive that slides out of the base housing when you release a catch. Both drives have a 28-msec seek time.

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All the hardware and software packages discussed here will provide you with the facilities for keep-

ing your data safe against theft or destruction, but there's no such thing as a bullet-proof system and humans are the weakest link in the security chain. Security experts repeatedly point out that the key to good security is a set of procedures that are neither lax enough to provide loopholes nor stringent and difficult enough to hinder you in your work. If your employees get lazy and don't change passwords often enough, or choose passwords that are easy to guess or find, your computer system becomes vulnerable. If the system administrator does not immediately invalidate the password of a terminated employee, he creates a gateway for a potential snooper. If you have antiviral programs and don't use them regularly, a worm may one day ooze its way into your system. You employ accountants to take care of your financial procedures; you should consider talking to a security consultant, or at least read some books on the topic of security, to help you take care of your data—which also represents money.

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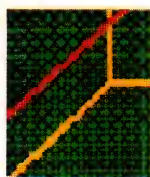
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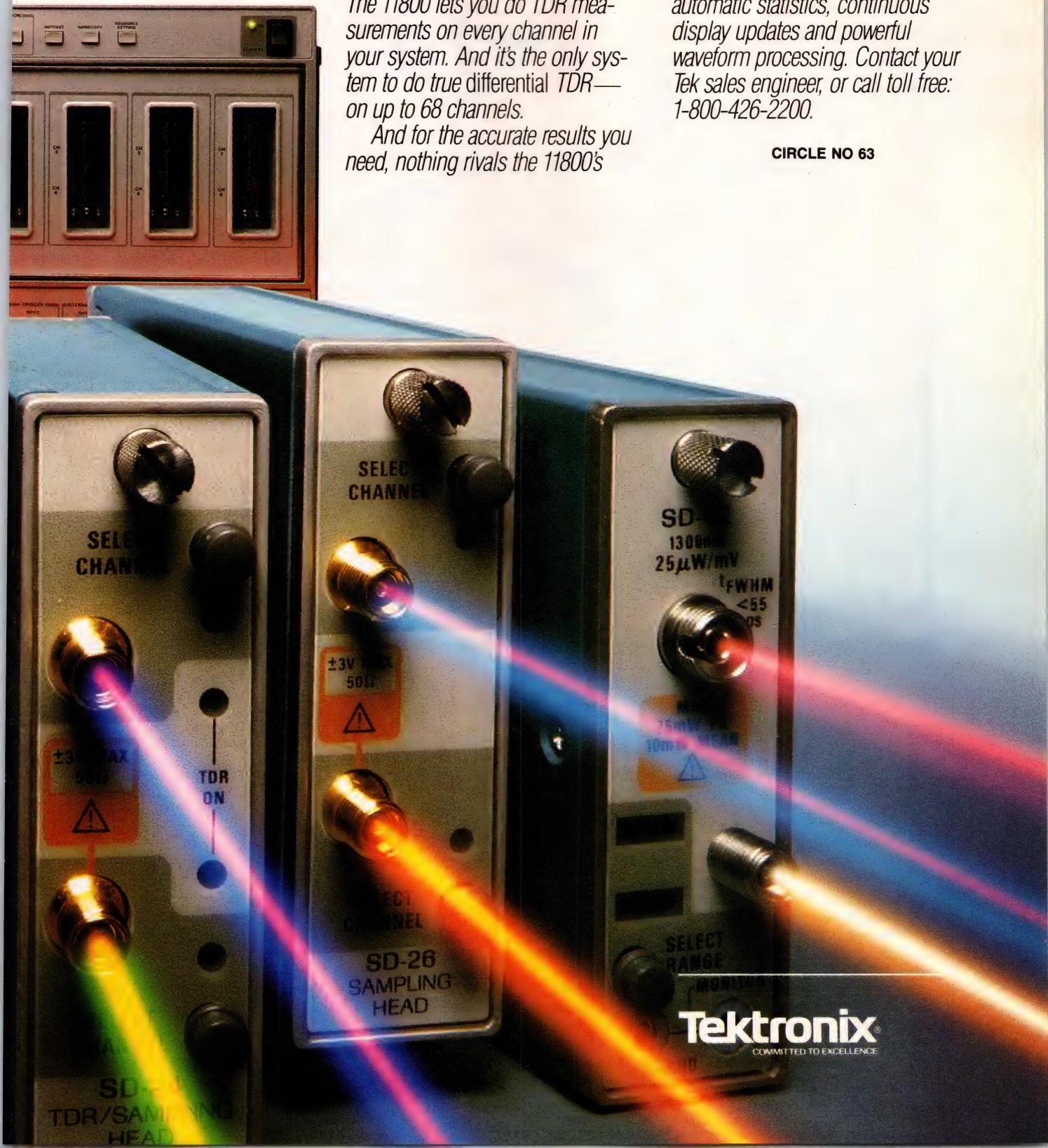
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Real-time kernels scarce for single-chip μ Ps



If you venture forth in pursuit of the lowest chip costs, you may end up in a realm almost bereft of formal, real-time software tools.

Charles H Small,
Associate Editor

Because single-chip μ Ps have vacuumed up many of the facilities that designers need for an embedded system into one inexpensive chip, single-chip μ Ps are an attractive option at the hardware level. Almost one-half of all embedded systems that use single-chip μ Ps must respond quickly and predictably to asynchronous inputs from the outside world. Therefore, these embedded systems are good candidates for real-time kernels. Unfortunately, even though a wide variety of third-party, real-time kernels and operating systems are available for standard μ Ps, far fewer formal, real-time tools are available for single-chip μ Ps.

This situation is particularly acute for 8-bit, single-chip μ Ps. The lack of formal, third-party, real-time tools for 8-bit, single-chip μ Ps forces most designers to roll their own real-time kernels (or executives, as they are sometimes called).

Using formal real-time tools with single-chip μ Ps might strike some engineers as overkill. After all, engineers have traditionally used a simple, synchronous polling loop for the small, fast programs that single-chip μ Ps usually run. But manufacturers of single-chip μ Ps have been installing more and more internal memory in their chips, in response to the need to accommodate ever larger applications. It's no longer a given that a single-

chip- μ P program will be so small and simple that a synchronous loop will suffice.

Some of the reasons for employing a real-time kernel instead of a polling loop for single-chip μ P programs are

- Polling loops are difficult to maintain. Even the slightest modification to one portion of the program can vary the execution time of the entire loop.
- Polling is often incompatible with interrupts. An interrupt presenting critical data may have to wait until the polling loop has made almost a complete cycle before the data gets processed. In the worst case, successive interrupts can overwrite, and thus destroy, critical



A real-time kernel must handle multiple, asynchronous interrupts. (Photo courtesy Wind River Systems Inc)

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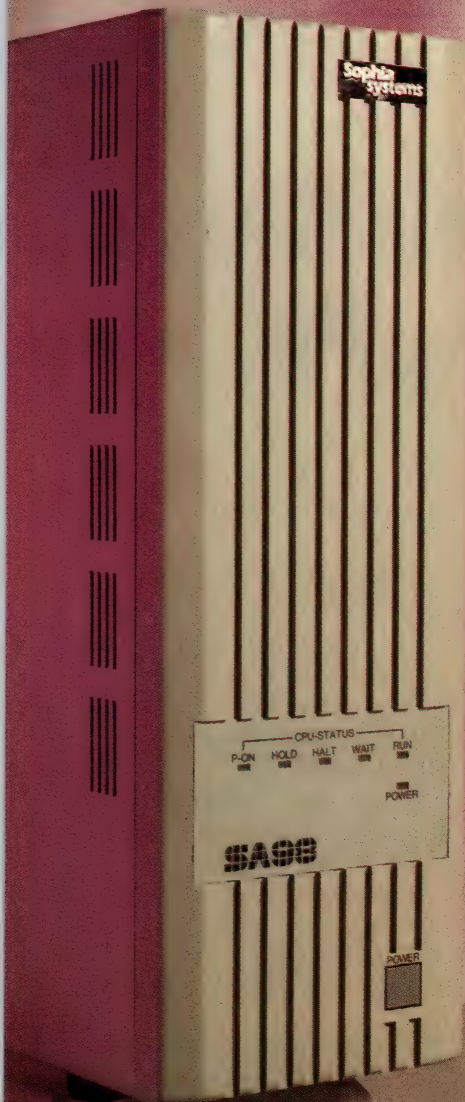
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TECHNOLOGY UPDATE

Real-time kernels

data before the polling loop processes them.

- As the number of interrupts a polling loop must manage increases, the loop's execution time becomes more and more variable from cycle to cycle. This variation obviously makes guaranteeing response times difficult.

- Polling loops waste time when they poll inputs that have nothing to say.

Therefore, a formal, real-time kernel begins to look attractive when your single-chip- μ P applications grow to the point where they require more than one programmer, must respond to more than a couple of interrupts, and are each divisible into more than three concurrent tasks.

Engineers seeking a real-time kernel for 8-bit, single-chip μ Ps face somewhat bleak prospects. Two vendors have recently withdrawn their 8051-family real-time kernels from the market. One of those vendors, Micro Computer Control, plans to redesign its kernel and reintroduce it this fall.

If the truth be told, 8-bit, single-chip μ Ps are tough nuts for real-time kernel designers to crack. Two



A real-time kernel orchestrates the operation of a data logger installed at this power station. (Photo courtesy United States Software Corp)

almost insuperable problems face kernel designers: first, most single-chip- μ P users would rather roll their own real-time executives than pay for one; second, the architecture and instruction sets of 8-bit, 1-chip μ Ps just don't suit multitasking as well as the architecture of standard μ Ps.

Writing your own real-time kernel is a challenging and satisfying

job that many competent software engineers would relish (Ref 1). Rolling your own kernel does present problems, however. In addition to the code, you must write and maintain your own documentation. Also, where third-party kernel vendors can supply drivers for many common peripheral chips and interfaces, you must write all your own drivers for your kernel. And

Pinning down the scope of a real-time kernel

Just what is a real-time kernel? Two industry pundits define real-time kernels as "... basic asynchronous solutions of limited functionality." However, real-time kernels don't come in liquid form, so calling them "solutions of limited functionality" doesn't clear up much confusion.

Actually, good real-time kernels don't have "limited functionality" either; they function quite well. If you spend the time to apply them properly, they can help you solve a certain range of knotty, embedded-system problems.

It's best to think of a real-time kernel as the core of a real-time operating system. Real-time kernels have facilities that allow you to parcel out the jobs your software must accomplish over a number of

relatively independent, autonomous tasks. In this way, you can reduce the complexity of your software design at the detail level, by distributing the processing load over a number of simple programs.

Specifically, real-time kernels have a supervisor that decides when, or in what order, each task will get control of shared system resources, such as the processor, memory, and I/O channels. The supervisor also manages communication between those tasks that must exchange data or control messages. Real-time kernels, on the other hand, lack many of the functions of a full-fledged, real-time operating system, such as disk and terminal I/O, file systems, human interfaces, local-area networking, and host-communication facilities.

TECHNOLOGY UPDATE

Real-time kernels

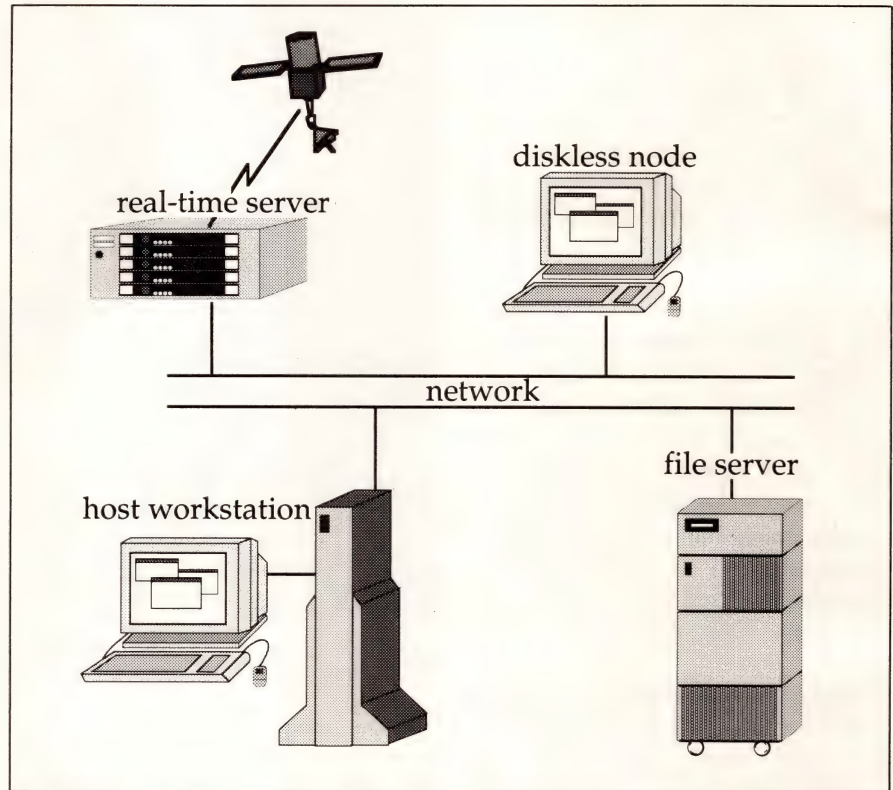
when your company adopts a new single-chip μ P, you must roll your system over onto the new architecture yourself.

Although cooking up your own arcane real-time system does have the highly desirable effect of designing in job security for its author, third-party kernels offer the advantage of having available a pool of trained programmers from which your company can hire. Also, third-party kernels often have users' groups and sources of public-domain software.

Real-time kernels need RAM

No matter who concocts the real-time kernel, single-chip μ Ps are far from ideal real-time engines. Even the newest, 8-bit, single-chip μ Ps are still rich in ROM and poor in RAM. New 8-bit, single-chip μ Ps may have as much as 32k bytes of ROM but only 512 bytes of RAM. Real-time kernels, unfortunately, need RAM.

Most real-time kernels allocate a separate stack in RAM for each task. A real-time kernel can theoretically use a single stack for multiple tasks, but cramming multiple, overlapping interrupts onto a single stack soon results in a corrupted nightmare. In addition to gobbling



Real-time kernels lack the file-handling and communications facilities of a full-fledged, real-time operating system. (Illustration courtesy Wind River Systems Inc)

up RAM with multiple stacks and usurping precious registers for pointers, real-time kernels also need a certain amount of RAM for their supervisor task's internal use for managing queues, lists, and message buffers.

Consequently, some real-time kernels originally written for standard μ Ps need so much RAM that they would require a single-chip μ P to operate in the so-called "large model" or "expanded model," rather than in the "small model." That is, some real-time kernels would require external memory rather than the single-chip μ P's internal memory. This forced operation from external memory dilutes the attractiveness of single-chip μ Ps, because it means tying up some of the single-chip μ P's limited, precious I/O ports as address and data lines to the external memory, adding chips and their attendant extra power consumption to your design, and slowing down program execution because of the increased time for memory operations. Not all designs can tolerate these liabilities.

Thus, most of the well-known

Real-time systems you can run on your IBM PC

Before embarking on a real-time design for a single-chip μ P, you might want to experiment with one of these real-time operating systems that run on the IBM PC. The SMX evaluation kit from Micro Digital Inc costs \$95, the OS-9000/386 professional system from Microware Systems costs \$950, and Quantum Software Systems' QNX operating system costs \$450.

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6402 Tulagi St
Cypress, CA 90630
(714) 891-2363

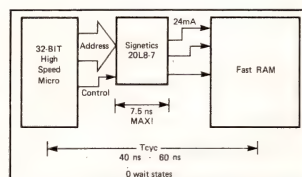
Microware Systems Corp
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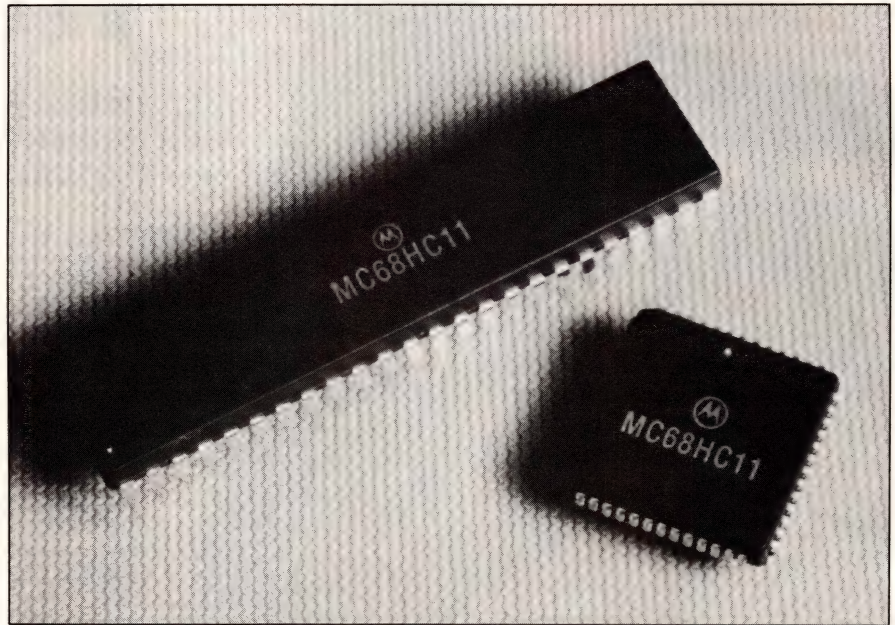
TECHNOLOGY UPDATE

Real-time kernels

real-time kernels aren't available for single-chip μ Ps. For example, Intel reserves its iRMK real-time kernel for its full-blown processors, such as the 80960 and 80386. For the firm's 8051 and 8096, Intel offers the simpler DCX real-time executive.

Aficionados of the 8051 can get a unique hardware/software development package from Forth Inc. Forth Inc strips Intel's ROM from an Intel EV80C51FA microcontroller evaluation board and replaces it with the 8051 version of its ChipForth kernel in ROM. ChipForth is a pre-ROMed version of the company's multitasking PolyForth. Along with the re-equipped evaluation board, you get an IBM PC software suite.

The resulting package, dubbed the cF8051, costs \$3750. Unlike the board's original ROM, the ChipForth ROM has upload and download facilities that allow it to communicate with the IBM PC host. The Forth compiler running on the IBM PC compiles your program directly into the evaluation



You can get a free real-time kernel for the 68HC11 from Motorola.

board's memory in one automatic step as you write it. Thus you can perform interactive, real-time development right on the 8051 evaluation board.

Harris can supply its RTX2000 Forth μ P as a μ P, or at higher cost, in the form of single-chip μ P, be-

cause the RTX2000 is only one element among many in the firm's semicustom-IC library. The company claims that compilers for high-level languages other than Forth will be available for the device.

The RTX2000 has no assembly language per se; it runs high-level

For more information . . .

For more information on the real-time kernels discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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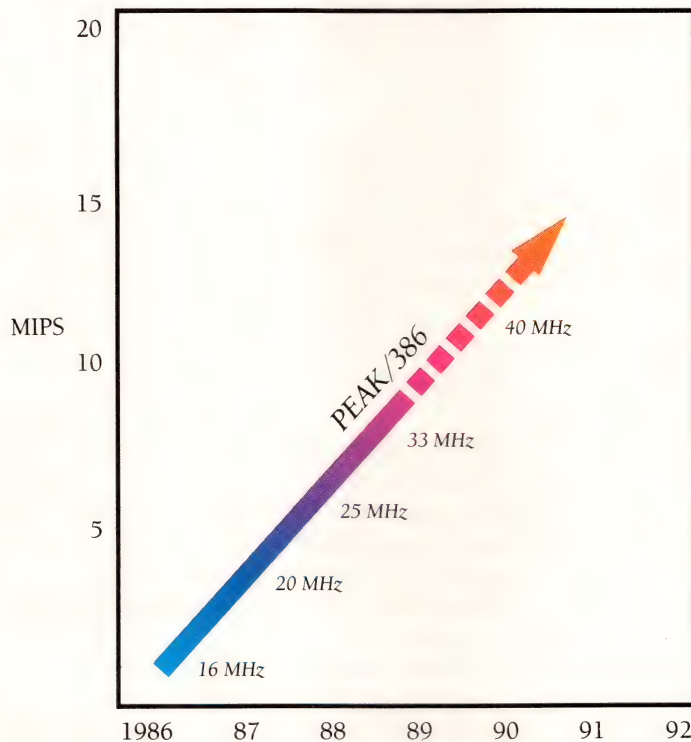
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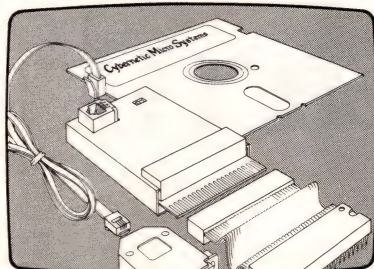
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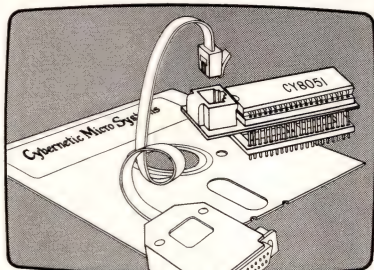
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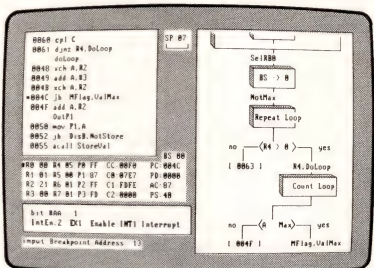
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DICE-51 \$495

This reduced-speed in-circuit 8051 debugger provides full access to I/O but will not run real-time. With the same user interface features as Sim8051 below, DICE-51 generates execution profiles during reduced speed execution. (CMOS and MIL also available.)



Sim8051 \$395

This software Simulator/debugger allows 'no-circuit' debugging of 8051 code on IBM-PCs. All Cybernetics 8051 debug tools offer multi-window source code displays, symbolic access to data, single key commands, breakpoints, trace, full speed and single step execution, execution profiler, and more.

Other 8051 tools include:

Cross Assembler \$195
8751 Programmer \$195-\$345
Debugger Demo Disk \$39



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TECHNOLOGY UPDATE

Real-time kernels

Forth directly. The processor's ability to execute Forth "words" directly leads to a nonpipelined architecture that provides benefits for real-time applications.

A Forth program, consisting of a string of Forth "words," is actually a list of named subroutines. Because calling subroutines is the native program-execution mechanism of Forth, these subroutine calls are implicit in a Forth program. Thus, the RTX2000 is optimized for subroutine calling and context switching in as little as a single cycle.

Most of the other new, 16-bit, single-chip μ Ps haven't yet acquired a real-time kernel. The 8096 is an exception.

US Software offers USX real-time executives for the 8051, 8096, and 68HC11, which cost \$1950 each. The development software for USX runs on an IBM PC and consists of a series of functions that you link in with your task code.

Software Environments Ltd multitasking executives for the 8051, 8096, and 68HC11 are compact enough to fit in the onboard RAM and ROM. The firm sells the executive's source code for a one-time fee of \$1950.

Motorola alone, among major firms, claims to have seen a recent upsurge in demand for real-time kernels for single-chip μ Ps. Motorola has responded to these demands in a unique fashion, by commissioning a real-time kernel for its 68HC11 that has an unbeatable price/performance ratio: the MCX11 real-time kernel, including the MCX11 source code and its manual, is free.

For the engineer determined to use a standard- μ P, real-time kernel with a single-chip μ P, a few hardware solutions to the single-chip- μ P selection problem are at hand. Certain single-chip μ Ps have standard

μ Ps as their core processor. Therefore, they can run the real-time kernels designed for their parent, standard μ Ps.

Examples of these standard-core, single-chip clones are the 64180, which has a Z80 core processor, and the 68070 and 68331 single-chip μ Ps, which have 68000 core processors. To customize a third-party, real-time kernel for these single-chip μ Ps, you need only write drivers for the single-chip μ P's onboard peripherals. Writing such custom drivers is a normal part of integrating a real-time kernel into any application—single-chip μ P or standard μ P.

All real-time kernel vendors have been approached to develop kernels for all the emerging RISC and embedded-system processors. Unlike their 8-bit cousins, the 32-bit processors that catch on in the market will probably spawn a fertile market for third-party software. Only time will tell which of these chips' architectures actually suits embedded real-time processing. **EDN**

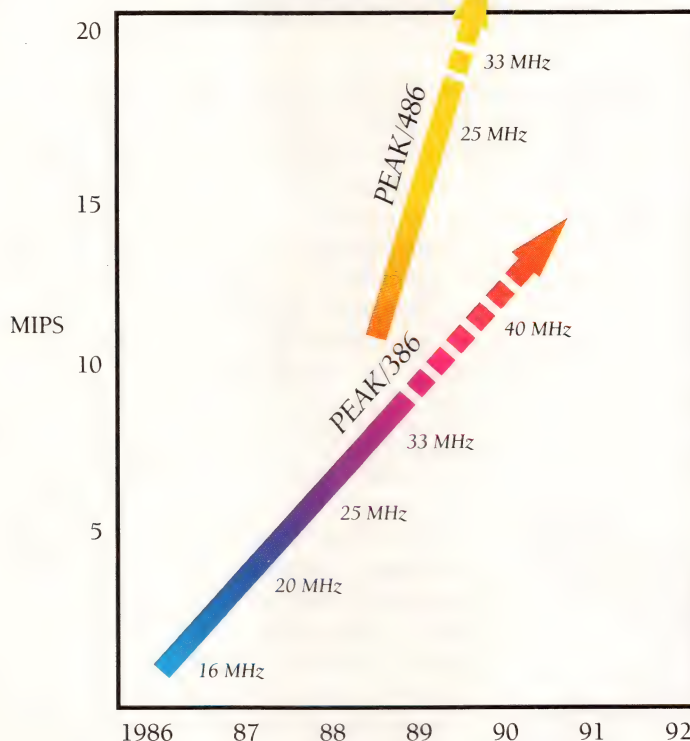
References

1. Ganssle, Jack, "Writing a Real-Time Operating System," *Circuit Cellular Ink*, January/February 1989, pg 45.

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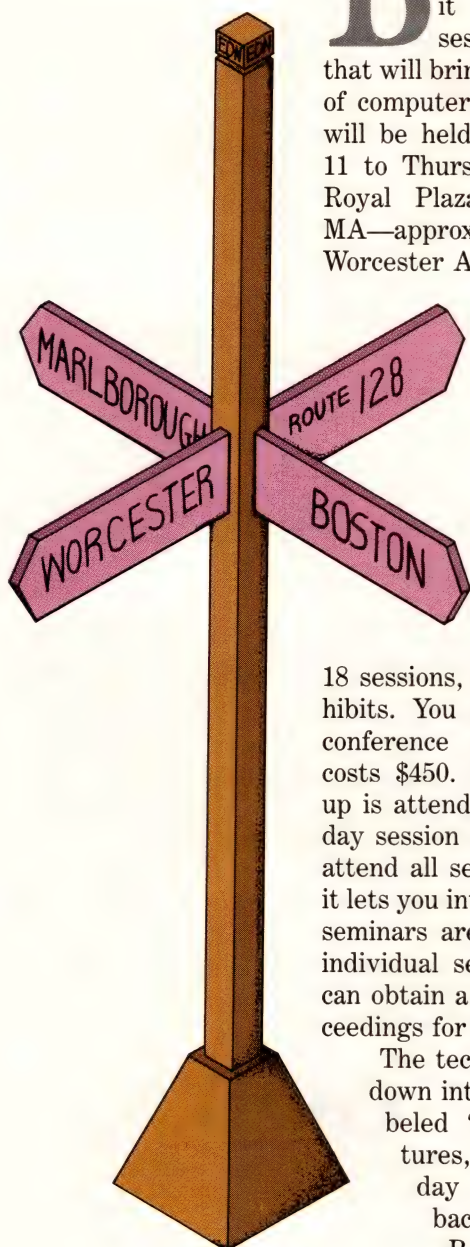
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Joan Morrow,
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Buscon East moves from New York last year to the Boston area this month, bringing with it its traditional grab bag of sessions and product exhibits that will bring you up to date in the field of computer-bus technology. The show will be held from Monday, September 11 to Thursday, September 14 at the Royal Plaza Hotel in Marlborough, MA—approximately 25 minutes from Worcester Airport and 45 minutes from Boston's Logan Air-

port. The show's organizers have anticipated the diverse needs of Buscon's attendees and have devised many ways for you to select exactly what you need. Option 1 gives you the works—admission to all six 4-hour seminars, all

18 sessions, and the more than 125 exhibits. You also receive a copy of the conference proceedings. This option costs \$450. For \$25 less, all you give up is attendance in the seminars. A 1-day session pass for \$245 allows you to attend all sessions on a given day, and it lets you into the exhibition. Individual seminars are priced at \$140 each, and individual sessions cost \$90 each. You can obtain a copy of the Buscon/89 proceedings for \$100.

The technical conference is broken down into three tracks. Track 1, labeled "Extending Bus Architectures," will begin with two half-day seminars that examine backplane bus design. Paul Borrill, chairman of the Mul-

tibus II and Futurebus committees, will cover the physical layer of backplane bus design and discuss the benefits and tradeoffs of existing standards.

Track 1 also includes six sessions that will be devoted to the next-generation architecture; personal-computer buses; the flexibility of the VXibus; STD Bus applications and performance; how to interface RISC and CISC processors on existing architectures; and how to meet military requirements for board-level products.

A seminar on the principles of system design using standard board-level products and one on just-in-time and quality-control manufacturing for board-level products will lead off the "System Technologies" Track 2. The six sessions in the track will cover a host of topics, among them the Intelligent Peripheral Interface (IPI) and related disk drives and controllers; how to implement data-acquisition hardware and software in automation and control applications; and the new generation of RISCs and its architectural issues. Another session will go over a new set of processor benchmarks and discuss the effectiveness of conventional benchmarks in general and how any new ones will fare. The two other sessions in Track 2 will detail opportunities in mixed-bus architectures and cover SCSI's command-set problems from the controller and drive manufacturers' point of view.

"Software Technology" is the focus of Track 3. Its first seminar will deal with the issues involved in real-time-system design and the tradeoffs between building and buying real-time operating systems. The other seminar will discuss what's involved in designing RISC proc-

BUSCON/89 EAST PROGRAM SCHEDULE

	TRACK 1 EXTENDING BUS ARCHITECTURES	TRACK 2 SYSTEM TECHNOLOGIES	TRACK 3 SOFTWARE TECHNOLOGY
MONDAY, SEPTEMBER 11	8:00 AM-12:00 PM SEMINAR 1001 BACKPLANE BUS DESIGN I	SEMINAR 1002 INTRODUCTION TO SYSTEM ARCHITECTURE FROM A BOARD- LEVEL PERSPECTIVE	SEMINAR 1003 DESIGNING REAL-TIME SYSTEMS
	1:00 PM-5:00 PM SEMINAR 2001 BACKPLANE BUS DESIGN II	SEMINAR 2002 JUST IN TIME AND TOTAL QUALITY CONTROL MANUFACTURING	SEMINAR 2003 APPLYING RISC TECHNOLOGY TO REAL-TIME APPLICATIONS
TUESDAY, SEPTEMBER 12	9:00 AM-11:00 AM SESSION 101 BRIDGING TO THE NEXT GENERATION ARCHITECTURE—VME TO NGA, MB II TO NGA, FUTUREBUS TO NGA, OTHER ISSUES	SESSION 102 SINGLE-USER DISK PERFORMANCE—UNSCRAMBLING THE SCSI COMMAND SET CONFUSION	SESSION 103 COMMUNICATING IN A HIGH- PERFORMANCE ENVIRONMENT: ETHERNET, FDDI, ETC
	2:00 PM-4:00 PM SESSION 201 THE CHANGING FACE OF PC BUSES EISA, MICRO CHANNEL, AT, NUBUS	SESSION 202 THE NEXT GENERATION IN DISK PERFORMANCE—IPI	SESSION 203 MULTIPROCESSING IN A REAL-TIME ENVIRONMENT
WEDNESDAY, SEPTEMBER 13	9:00 AM-11:00 AM SESSION 301 VXI BUS—INSTRUMENTATION AND BEYOND	SESSION 302 MIXING BUS STANDARDS—AT ON VME, AT ON MB II, STD ON MB II	SESSION 303 REAL-TIME ADA
	2:00 PM-4:00 PM SESSION 401 SPOTLIGHT ON STD BUS APPLICATION/PERFORMANCE	SESSION 402 NEW MACHINES, NEW BENCHMARKS—MEASURING SYSTEM PERFORMANCE	SESSION 403 GRAPHICS AND REAL-TIME SYSTEMS XWINDOWS, GKS
THURSDAY, SEPTEMBER 14	9:00 AM-11:00 AM SESSION 501 SATISFYING MILITARY REQUIREMENTS FOR BOARD-LEVEL PRODUCTS	SESSION 502 BUSING RISC ARCHITECTURES	SESSION 503 APPLYING DEVELOPMENT TOOLS TO A REAL-TIME ENVIRONMENT
	2:00 PM-4:00 PM SESSION 601 EXTENDING BUS PERFORMANCE	SESSION 602 PUTTING DATA ACQUISITION HARDWARE/SOFTWARE TO WORK	SESSION 603 RUN-TIME HYBRID SOFTWARE ENVIRONMENTS—UNIX, DOS, REAL- TIME, INCLUDING CONCURRENT/LINX

errors into real-time systems. In the Track 3 sessions, you can learn about the Ada language and real-time Ada tools for use in military and commercial applications; how to implement graphics in real-time systems; and real-time development and testing tools, symbolic and source-level debugging facilities, and high-level languages.

For more information on Buscon/89 East, you can contact CMC, 200 Con-

necticut Ave, Norwalk, CT 06856; phone (203) 852-0500 or FAX 203-838-3710. To register for seminars or sessions, call (800) 243-3238, ext 232. **EDN**

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The 2- and 4-way set-associative organizations of cache memory reduce thrashing when programs jump between multiple main-memory addresses at the same page offset. This feature is particularly useful when executing programs where successive accesses tend to be random, and the data is evenly spread over the system-memory map, as is often the case in databases.

The cache controller also offers copyback in addition to write-

through and posted writes for maintaining main-memory coherency with the cache. Although the write-through approach found on other cache controllers guarantees real-time coherency, this approach reduces system speed because writes to the cache are simultaneously written to main memory, tying up the main memory when other bus masters could be using it.

The write-through approach is often used because it prevents a remote master from reading a location in main memory that has been updated in the cache but not copied back into main memory. In an actual system with large amounts of main memory, the probability of a remote master accessing a location presently in the cache is small, and the probability of the data being inconsistent between the system and cache memory is even smaller.

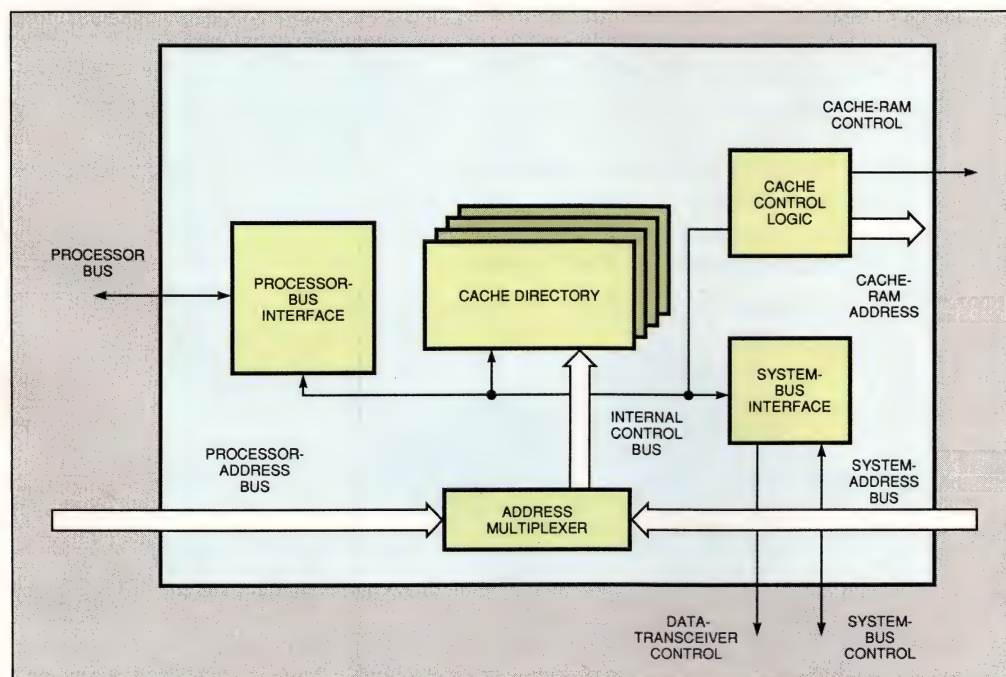
Using the copyback mode, the C395e provides correct data on

those occasions when a remote master attempts to read inconsistent data. The 395e does this by "snooping" for reads by any remote master of a main-memory address that is both present in the cache, and that has data inconsistent with the cache. If the controller finds such a case, it disables the main memory and provides the data out of the cache.

The C395e requires only the addition of four 8-bit transceivers and a RAM for use with an 80386. You can order samples of 20- and 25-MHz versions in October, with full production at the end of 1989. In early 1990, 33-MHz versions will be available. The 25-MHz 164-lead JEDEC quad flatpack costs \$174 (100).—**Doug Conner**

Matra Design Semiconductor, 2895 Northwestern Pkwy, Santa Clara, CA 95051. Phone (408) 986-9000. FAX 408-748-1038.

Circle No 731



Supporting as much as 256k bytes of cache memory, the MDS-C395e cache controller also offers 4-way set-associative organizations. To maintain coherency between the cache memory, the device offers copyback, write-through, and posted writes.

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```
> Display trace memory (in structured format)
Enter starting address(hex): 0
0001: Arbitration /80
0003: Select w.ATN /C0
0006: Message-Out/CO(Identify)
0007: Command /T2(Inquiry) 00 00 00 00 00 43 4F 4E 4E 52 20 20
0008: Data-In /00 00 01 01 29 00 00 00 43 4F 4E 4E 52 20 20
0010: 43 70 33 34 30 20 28 34 30 60 62 20 33 2E 35 29
0020: 20 30 34 20 42 30 31 33 54 42 20 20 20 20
0038: Status /00
0039: Message-In /00
0039: Bus free
003F: Arbitration w.ATN /80
0041: Select w.ATN /C0
0044: Message-Out/CO(Identify)
0045: Command /08(Read) 00 00 10 01 00
0048: Message-In /04(Discard)
004C: Bus free
004C: Arbitration /40
0050: Reselect /C0
0052: Message-In /80(Identify)
0053: Data-In /00 00 00 00 12 34 56 79 12 34 56 7A 12 34 56 7B
0063: 12 34 56 7C 12 34 56 7D 12 34 56 7E 12 34 56 7F
```

```
> Display trace memory (in BINARY format)
Enter starting address(hex): 0
TMR: BSY SEL ATN RST MSG I/O C/D DATA ParErr Exp Time Diff (ns)
0000: A - - - - - 01 - - - - 00 0 000
0001: A - - - - - 01 - - - - 00 21 750
0002: A - - - - - 00 - - - - A 00 11 250
0003: A - - - - - 00 - - - - 00 269 250
0004: A - - - - - 00 - - - - 00 145 500
0005: A - - - - - 00 - - - - 00 129 000
0006: A - - - - - 00 - - - - 00 129 000
0007: A - - - - - 00 - - - - 00 129 000
0008: A - - - - - 00 - - - - 00 138 750
0009: A - - - - - A 00 - - - - 00 180 000
000A: A - - - - - A A 00 - - - - 00 173 000
000B: A - - - - - 00 - - - - 00 72 250
000C: A - - - - - 01 - - - - 00 5 455 100
000D: A - - - - - 01 - - - - 00 29 950
000E: A - - - - - 00 - - - - A 00 13 250
000F: A - - - - - A 0A - - - - 00 269 250
0010: A - - - - - A 00 - - - - 00 155 250
0011: A - - - - - A 00 - - - - 00 138 750
0012: A - - - - - A 20 - - - - 00 138 750
0013: A - - - - - A 01 - - - - 00 138 750
0014: A - - - - - A 00 - - - - 00 138 750
0015: A - - - - - A0 - - - - 00 431 350
```

[415] 363-0667

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1755 E. Bayshore Road, 18A
Redwood City, CA 94063

CIRCLE NO 9

PRODUCT UPDATE

Multiprocessor DSP board offers 50-MIPS performance

The VE-32C-01V 4-processor-VMEbus DSP board targets computationally intensive applications such as image processing, graphics, and finite element analysis. Based on the AT&T DSP32C processor, the single-slot board executes a 1024-point FFT algorithm in 1 msec. Each of the four processors can perform a 3×3 matrix multiplication in 2.2 μ sec. The board achieves peak-performance specifications of 50 MIPS and 100M flops.

The DSP32C DSP μ P includes 1536 32-bit words of RAM on chip. The VMEbus board also supplies an additional 32k to 128k bytes of zero-wait-state static RAM for each of the four processors. On-chip serial ports provide a 6.25M-bps communications link that chains the four processors together. The daisy-chained signal is also accessible on the VMEbus P2 connector.

Separate 16-bit parallel input and output ports operate with transfer rates as fast as 10M words/sec. The input port also includes a 1024-word FIFO buffer. The ports connect both to the VMEbus P2 connector and to dedicated front-panel connectors. A matrix switch routes information between the four proces-

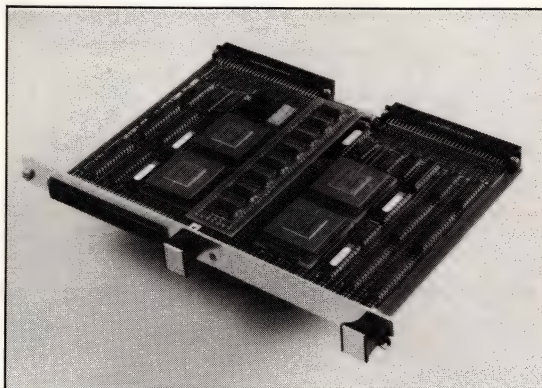
sors and the two ports. The 6U board serves the role of a VMEbus slave and supports 24 address and 16 data lines. The device can activate four of the seven VMEbus interrupt levels.

An assembler, a linker, a simulator, and a compiler make up the basis of available support software. The board also comes with a C language applications library that includes math, matrix manipulation, signal processing, image processing, and graphics routines. The manufacturer also offers Unix drivers that integrate the DSP board with Sun workstations.

You can use more than one of the boards to serve applications that demand higher performance. A 16-board implementation achieves a peak performance of 1.6G flops. The board costs \$7650 (10) with 32k bytes of RAM per processor installed. Delivery, four to six weeks ARO.—**Maury Wright**

Valley Enterprises Inc, RD #4,
Rt 309, Tamaqua, PA 18252. Phone
(717) 668-3737.

Circle No 730



A 1024-point FFT algorithm executes in 1 msec on the DSP32C-based 4-processor VMEbus board. The VE-32C0-01V can perform at a peak of 50 MIPS and 100M flops.

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Nonvolatile memories

Michael C Markowitz,
Associate Editor

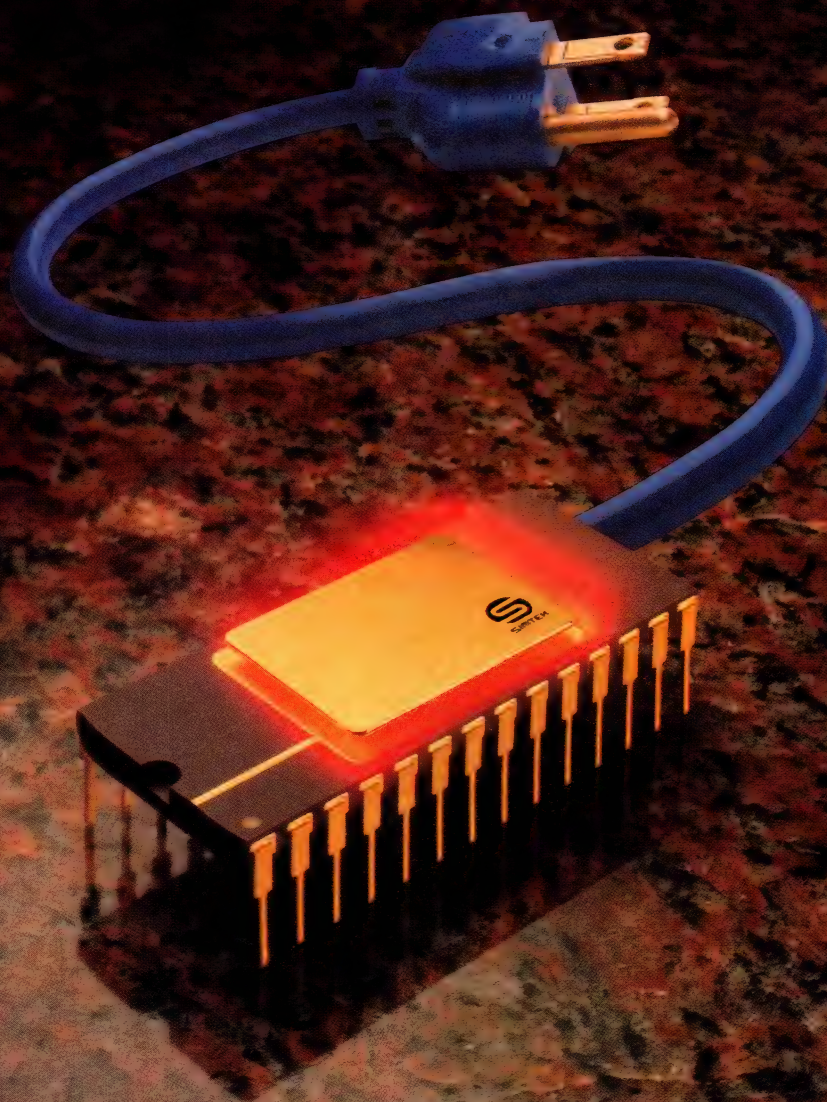
A host of alternatives confronts you in trying to evaluate and select nonvolatile memories. The choices cover a phenomenal range of bit densities—starting as low as four bits per device and extending to 8M bits per chip. And lest you thought that memories couldn't get much more dense, 16M-bit read-only memories (ROMs) were introduced at the International Solid-State Circuits Conference (ISSCC) in February.

One important performance criterion is read-access time. Write-cycle time and endurance are also critical if you need to write information into the memory rather than have the vendor do it. These three specifications can also swing between wide ranges. Read-access times can be as low as 15 to 20 nsec or into the microsecond range. Write and erase cycles can take from a few tens of nanoseconds to a few seconds. The ability of a reprogrammable nonvolatile memory to survive repeated write cycles extends from 100 cycles to better than 1,000,000 cycles.

Cost, of course, is an obvious consideration. If you only need four bits of nonvolatile data storage, there are devices that will serve your purpose—but at a price that may prod you to consider alternatives. Cost per megabit for various types of nonvolatile memory ranges from less than \$4 per megabit to \$31 million per megabit.

At the low end of the nonvolatile-memory price-and-flexibility scale are ROMs, which you purchase from the vendor already programmed. These nonvolatile memories are often used as the

With such a wide range of nonvolatile-memory types and performance capabilities available, it can be a daunting task to find the right one for your application. As a result, it helps to have a good idea of what your choices are, so you can avoid some of the confusion about what a memory can or cannot do.



Pull the plug on nonvolatile memories without losing data. (Photo courtesy Simtek Corp)

You can find nonvolatile memories in densities from 4 bits to 8M bits at prices that range from \$4 per megabit to—believe it or not—\$31 million per megabit.

boot memory of computers or for look-up tables. ROMs are frequently used in cost-driven systems, where program stability and high volume demand a dense, inexpensive, permanent memory. But because ROMs aren't reprogrammable, if you need to change the memory's contents, you must replace the ROM.

To purchase a ROM, you provide a vendor with a truth table describing the circuit function you want to implement. The vendor converts your truth table to a mask pattern, which specifies the metallization of the ROM. If the metal exists for a particular bipolar-junction transistor, the metal connects the emitter to the appropriate output line, and the transistor stores a 0. If the metal doesn't exist, the emitter floats, and the transistor stores a 1.

The mask step customizes the ROM for your application and prevents the vendor from offering the chip to the commercial market. Thus, ROMs have either nonrecurring engineering charges (NRE) or minimum volume requirements and sometimes both. NREs are generally in the \$2500 range, and minimum orders start at 1000 pieces. On the other hand, densities as high as 4M bits are available, and, as a group, ROMs have the lowest cost—starting around \$3.60 per megabit and going up to just under \$11 per megabit.

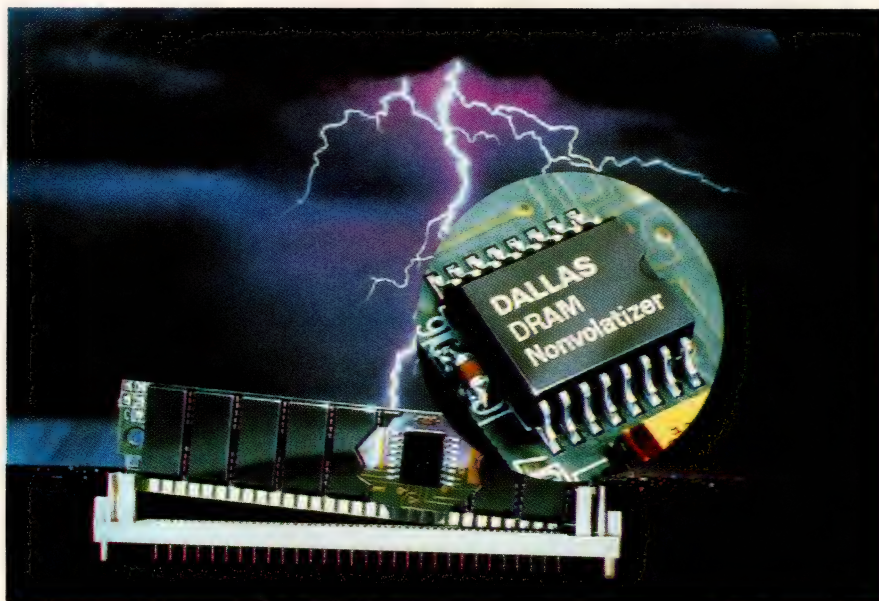
Most ROMs won't set any speed records, however. Read-access time is in the 100- to 250-nsec range. In cases where your processor or controller is looking for faster access, you'll need to use a faster memory family or add wait states to your ROM application.

Because of the mask step of ROMs, delivery of your chips is typically six to 12 weeks after you place your order. However, in this age of shrinking time to market and JIT (just-in-time) delivery, you may need a nonvolatile memory with a shorter leadtime. Two types of nonvolatile memory address this need. Both fuse-link PROMs and one-time-programmable (OTP) devices let you stock memories that can sit in your storeroom and that you program, once, as the need arises.

Fuse-link PROMs are generally bipolar, although some vendors are starting to provide BiCMOS devices. Bipolar PROMs are relatively fast and provide good radiation immunity, but they're also power hungry and, because of heat dissipation, limited in density. Testing, too, is a problem with PROMs. Because you don't want to blow a fuse to test it, you must take it on faith that the fuses work and limit your testing to the peripheral circuitry. PROMs have historically been used for storing macros and programs and in engine-control units; but, as high-speed EPROMs evolve, many of these applications are being handled by fast EPROMs and their siblings, the OTP memories.

OTP memories are EPROMs (erasable programmable read-only memories), but instead of being packaged in expensive windowed ceramic packages, OTP devices come in plastic packages. Without a window to let UV light reach the die, OTP memories—as their name states—don't have the reprogrammability feature of EPROMs. Because you needn't worry about removing OTP memories for reprogramming, you can even pur-

A controller chip can switch to a backup energy source and manage memory refresh for a DRAM—as long as the energy source survives.





Flash memories can be as dense as EPROMs, but they offer in-circuit block- or chip-erase capability.

chase them in surface-mount packages. OTP memories offer relatively inexpensive, permanent nonvolatile memory and have short leadtimes.

One type of OTP device is similar to a ROM. A family of devices that Advanced Micro Devices calls ExpressROMs are not true ROMs in that they are not *mask* customized. AMD manufactures these wafers using their standard EPROM process, except for the passivation layer. For ExpressROMs, this layer is a low-cost nitride topside—rather than the more expensive topside that permits UV erasure—and protects and seals the die. AMD programs the die at wafer sort and then tests the devices before you receive them. Because there is no mask step, there are no NRE charges. To program an ExpressROM, you send either a JEDEC (Joint Electron Device Engineering Council) program file or two identically programmed JEDEC-standard EPROMs to AMD, and it will program the chips—minimum order 5000—to your specification in about four weeks.

Stepping up a notch in flexibility and cost, EPROMs

are devices that come in a ceramic package with a quartz window. The window provides access for UV light to erase the information programmed into the EPROM. Because a single transistor is the storage element, the memory can be made very dense. Like ROMs, EPROMs are available in densities to 4M bits, and 8M- and 16M-bit devices are in the development phase.

As long as you don't need to rewrite the data often, there's likely to be an EPROM with a speed that satisfies your needs at a cost between \$14 and \$580 per megabit. Older EPROMs access data in speeds above 100 nsec, but a new generation of the memories takes advantage of design tricks and performance optimizations to achieve data-access times faster than 25 nsec. Texas Instruments announced an EPROM with a burst-mode configuration that achieves a high memory bandwidth via a statistical, cache-like methodology at this year's ISSCC. Cypress specifies its 4k- and 16k-bit registered PROMs—the company calls its EPROMs PROMs because they're available in PROM-standard pinouts—at 10- and 12-nsec clock-to-output delays. Some of Cypress's 16k-bit nonregistered PROMs operate with 20-nsec clock-to-output delays.

However, EPROMs do have a few drawbacks. First, although EPROMs are erasable and reprogrammable, this process is time consuming (see **box**, "The physics behind reprogrammable chips"). You must first remove the EPROM from your system, then expose the device to UV light for about 20 minutes before reprogramming it using an EPROM programmer. As previously mentioned, the UV-erase feature necessitates that EPROMs be packaged in expensive ceramic packages with quartz windows. Also, you must prevent against accidental erasure by obscuring the window in your system. And, because you must be able to remove the chip to reprogram it, you must socket an EPROM.

Use an EPROM if you can erase it all

Another limitation inherent to using EPROMs is your inability to selectively erase memory locations. You must erase either every location in the memory array or none of them. This restriction makes EPROMs ineffective memories for *data* storage. But these chips are viable as storage elements for applications such as maps, tables of quasipermanent data, and programs in which the stored information changes infrequently.

The limited endurance of EPROMs is another potential drawback. Because you program EPROMs with the hot injection of high-energy electrons through the

Most EPROMs are also available as OTP memories—low-cost variations that substitute plastic packages for more expensive windowed ceramic packages.

oxide, the memory cell deteriorates with use. Most EPROMs are specified to withstand 100 write cycles, although some vendors specify their devices to 1000 write cycles by using process-selection criteria. For applications in which you use the chip for infrequently changed *program* storage, 100 write cycles should be sufficient. But if you want to use the memory for storing frequently altered data, the EPROM is not a good choice.

If you need nonvolatile *data* storage, the full-featured EEPROM (electrically erasable programmable read-only memory) is a better choice than the EPROM. The EEPROM lends itself to applications such as the storage of calibration constants or PABX configuration data—applications in which some, but not all, of the information is likely to change over time.

Most EEPROMs are specified to endure 10,000 write cycles, although a number of manufacturers will select devices that will survive 100,000 or even 1,000,000 write cycles. But the significant advantages of EEPROMs are their in-circuit reprogrammability, generally using only a 5V supply, and their byte-erase capability.

Do you want charge pumps or more bits?

The design techniques that provide the EEPROM with its advantages are also responsible for its drawbacks. Because of the chip area taken up by the charge pumps that allow 5V-only operation and the circuitry that permits byte erasure, EEPROMs are significantly larger than EPROMs at comparable bit densities. As a result, EEPROMs—at costs ranging from \$180 to

The physics behind reprogrammable chips

Understanding the physics behind the programming and erasing mechanisms of EPROMs, EEPROMs, and flash memories isn't necessary to use these devices, but it can give you insights into why the memories achieve different densities and how they fail.

The EPROM offers a floating gate sitting on an oxide film about 350Å above the channel separating the source and drain of a transistor. The control gate of the device is above the floating gate. To program an EPROM cell with a 1, the programmer applies about 20V to the control gate and drain. The resulting channel current contains high-energy, or hot, electrons that flow through the insulating SiO₂ layer to the floating gate. When you drive the gate with a 5V supply, the negative charge on the floating gate keeps the device off. Exposing the programmed EPROM to UV light with a wavelength centered around 253.7 nm neutralizes the charge on the floating gate and

erases the EPROM.

The programming of an EEPROM takes advantage of an effect known as Fowler-Nordheim tunneling. This effect describes how a strong electric field can induce low-energy electrons to tunnel through a thin oxide and into the floating gate. As with EPROMs, you program an EEPROM by applying a high voltage—often generated on-chip by charge pumps—on the control gate. Capacitive coupling induces the voltage on the floating gate, which creates the electric field across the thin oxide. The tunneling current of about 1 nA that results programs the cell with a smaller cumulative charge than that found on the EPROM and lets the EEPROM cell conduct current in either programmed state. A select gate isolates the EEPROM cell from the other cells in the array and sends the cell's data to a sense amplifier when the select gate is enabled.

It is this select gate that takes up silicon area and limits the den-

sity of EEPROMs. The select gate permits byte erasure, which is, in effect, just a write operation. Burning an EEPROM involves grounding the program line for a row and then raising the column lines to the high programming voltage to match the data pattern that you want to load.

Flash memories are something of a hybrid of the two approaches. With most flash memories, you write data into the flash cell using hot-electron injection, as though you were writing a EPROM. Erasing flash memories utilizes the Nordheim-Fowler tunneling mechanism: You create an electric field by grounding the control gate and applying a high voltage to either the transistor's drain or source. In general, flash memories don't have a separate select gate—either they don't have one at all, or the select gate is part of the control gate. Therefore, flash memories don't have byte-erase capability.

\$1500 per megabit—are more than three or four times as expensive as EPROMs. Also, EEPROMs aren't capable of the same bit densities as are EPROMs, although the two device types offer comparable read-access times.

Another nonvolatile-memory alternative is relatively new and—as is often the case when a few competitors surface with something new—is creating confusion. Flash memories approach the density of EPROMs at a slight cost premium and offer the in-circuit erasure and reprogrammability of EEPROMs. Some manufacturers call their devices flash EPROMs and others call theirs flash EEPROMs, but there's little agreement about what the difference is. The only feature common to all flash memories is that they offer fast, in-circuit erasure of either a sector or the whole memory. The

name flash, in fact, was coined to describe this high-speed bulk-data erase.

To illustrate the divergent descriptions of flash EPROMs and EEPROMs, Texas Instruments claims that, since all of the flash devices are electrically erasable, they should all be called flash EEPROMs. TI claims that the flash EPROM moniker could be a marketing ploy to capitalize on the relative popularity of EPROMs over EEPROMs. Both Atmel and TI suggest that some vendors might name their flash devices for the type of socket they are trying to fill—those chips with EPROM-compatible pinouts are flash EPROMs; those with EEPROM-compatible pinouts are flash EEPROMs. Seeq claims the distinction is that whereas a flash EPROM is only programmable at room temperature, a flash EEPROM is programmable over the

TABLE 1—NONVOLATILE MEMORY VENDORS

COMPANY	ROMs	PROMs	ONE-TIME-PROGRAMMABLE MEMORIES	EPROMs	EEPROMs	FLASH MEMORIES	OTHER TYPES
AMD	•	•	•	•	•	•	
ATMEL				•	•	•	
CATALYST				•	•		NONVOLATILE SRAM
CONTROLEX							CORE
CYPRESS			•	•			
DALLAS							DRAM, SRAM
EXEL					•		
FUJITSU		•	•	•			
GOULD/AMI	•						
HITACHI				•	•		
INTEL				•		•	
ICT				•	•		
KRYSALIS							FERROELECTRIC RAM
MICROCHIP	•		•	•			
MITSUBISHI	•		•	•	•		ELECTRICALLY ALTERABLE ROM, VERSATILE ROM
OKI	•		•	•	•		
NATIONAL		•		•	•	•	
NEC					•		
RAMTRON							FERROELECTRIC RAM
RAYTHEON		•					
SEEQ				•	•	•	
SGS	•		•	•	•		SRAM
SHARP	•		•	•			
SIERRA					•		ASICs
SIGNETICS		•		•			
SIMTEK					•		NONVOLATILE RAM
TEXAS INSTRUMENTS			•	•		•	
TOSHIBA	•		•	•		•	
WAFERSCALE				•		•	
WHITE					•		
XICOR					•		NONVOLATILE SRAM

EEPROMs are more expensive than EPROMs, but they feature in-circuit byte-erase and program capability.

entire operating temperature range. Intel manages to sidestep the issue by calling its parts flash memories.

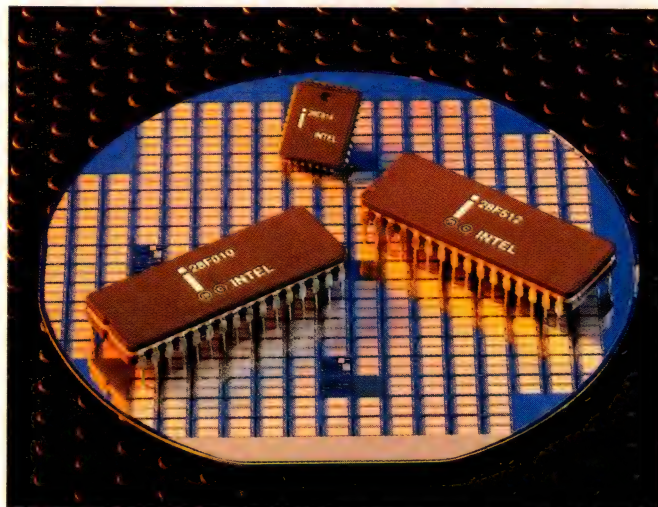
In addition to the characteristics that each of these vendors allude to, there are a number of others that you can use to differentiate among the flash offerings. Some devices are 5V programmable; others trade charge pumps for additional density and therefore need both 5V and 12V supplies. A number of flash memories have 100 or 1000 write-cycle endurance; others are capable of more than 10,000 write cycles.

Most EPROMs require both a 5 and a 12V supply, EEPROM parts generally only need the 5V supply, and flash memories can fit in either category. EPROMs are the most dense of the three technologies. You can buy 4M-bit EPROMs, but the highest density EEPROM you can buy is only 256k bits. As something of an intermediate technology, 1M-bit flash memories are available. In read-access speed, both EPROMs and EEPROMs are available in high-speed versions that can present valid data in under 50 nsec. Such flash devices are under development.

A final comment on the differences among the three memory families. A reflection of a memory's density and manufacturability is its cost. According to data collected by In-Stat (Ref 2), high-volume pricing of EPROMs runs between \$8.80 and \$56 per megabit. EEPROMs cost between \$160 and \$320 per megabit and are only available in 512k- and 1M-bit versions as modules. Flash memories occupy a midrange, costing between \$27 and \$320 per megabit.

For the end user, the major differences among EPROMs, EEPROMs, and flash memories are that both EEPROMs and flash memories offer in-circuit erase and program. EPROMs require that you remove the chip from the circuit, expose it for 20 minutes to UV light, reprogram with a programmer, and reinsert the IC. Additionally, whereas EEPROMs offer the ability to choose which byte you want to erase, erasing EPROMs is an all or nothing proposition, as are most flash memories. However, Seeq and National (through a joint licensing agreement) and Atmel do offer flash memories that let you erase on a sector-by-sector basis.

One potential danger in using some flash memories is overerase. When you erase a flash memory, you deplete charge from the memory cells. But if you remove too much charge, you'll create what one vendor described as a WOM (write-only memory). Flash memories require that as the first part of your erase algorithm, you program all the bytes to data 00_h to equalize the charge on all transistors. Your erase algo-



Although vendors can't agree on the differences between flash EPROMs and flash EEPROMs, it's important to understand the distinctions among the various devices.

rithm then controls the removal of charge from the transistors for a specified length of time. If you "over-erase" the memory or any of its cells, you render the chip unprogrammable. According to Intel's "Guide to Flash Memory Reprogramming," cell depletion occurs after 10 sec, whereas the erase operation is specified at 10.5 msec. Therefore, as long as you exercise good design practice, you needn't worry about creating WOMs.

Low cost reflects manufacturability

In addition to those memories already discussed, you can also choose among a number of other nonvolatile-memory types. Nonvolatile static RAMs (SRAMs) are SRAMs with a shadow EEPROM. This memory-cell redundancy limits the density of nonvolatile SRAMs and makes these chips very expensive. They work like SRAMs until you want to save data in the EEPROM. You can load information into the nonvolatile SRAM by sending it a Store instruction. This instruction can be sent either by signaling an input pin or by executing a software sequence that initiates the Store instruction and transfers the information from the nonvolatile memory's SRAM array into the EEPROM array, typically in 10 msec. You can load data back into the SRAM automatically on power-up or by using the hardware or software Recall instruction.

The major limitations of nonvolatile SRAMs are cost, density, and speed; but a start-up company, Simtek, is making improvements in all three areas. Simtek's nonvolatile SRAMs use SNOS (silicon nitride oxide



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For programming, most flash memories use the hot-electron-injection technique, like EPROMs, but a few use Fowler-Nordheim tunneling, like EEPROMs.

Manufacturers of nonvolatile memories

For more information on nonvolatile memories such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

Advanced Micro Devices
901 Thompson Pl
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Pocatello, ID 83201
(800) 468-5310
Circle No 658

NEC Electronics
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FAX 408-436-4200
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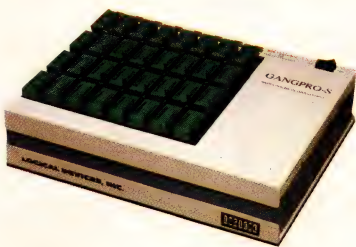
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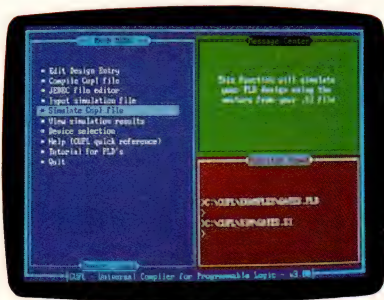


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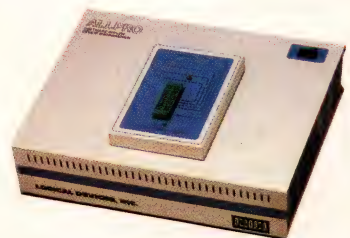
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Nonvolatile SRAMs combine SRAMs and EEPROMs on a single chip and let you save data temporarily in SRAM or permanently in EEPROM.

semiconductor) technology to store charge on the silicon nitride oxide insulator rather than on the conducting polysilicon floating gate. The SNOS technology, along with a few design tricks, effects an order-of-magnitude improvement in nonvolatile-SRAM cost—from \$7000 to \$780 per megabit; a 16-fold increase in density—from 4k bits to 64k bits; and 5 to 10 times faster read-access times—from 200 to 300 nsec to 35 nsec.

Even more expensive, slower, and less dense than nonvolatile SRAMs but capable of providing radiation hardness and operating under extreme temperatures are nonvolatile memories made of ferrite cores. You can use these memories in applications that cannot utilize other types of memories because of the potential for extreme conditions. You'd have a tough time justifying the expense of core memories in cost-sensitive applications. The price of the memories ranges from \$307,000 to \$31 million per megabit, although the largest ferrite-core memory is only 512 bits. But there are applications, such as nuclear power plants and down-hole drilling, in which you need the capabilities of these devices.

Ferroelectrics has existed for a while but may now be on the verge of fruition. This technology involves using a thin-film ceramic to form capacitors that sit above the conventional memory cell. To achieve higher density, these ceramic capacitors ultimately will replace rather than supplement memory cells.

Ferroelectric memories have the potential to offer the speed of SRAMs, the density of dynamic RAMs (DRAMs), and the nonvolatility of EEPROMs. However, the current generation of evaluation units, which feature read- and write-access times exceeding 200 nsec and densities less than 4k bits, doesn't seem much of a threat to SRAMs, DRAMs, or EEPROMs. And the start-up companies making ferroelectric RAMs are chasing a moving target. To survive, vendors must approach the density and performance of existing nonvolatile memories at a reasonable cost. The advantage of ferroelectrics is that it holds the promise of merging volatile and nonvolatile memory types.

Using existing technology, Dallas Semiconductor and SGS-Thomson have brought nonvolatility to SRAMs. To protect SRAM applications, these companies offer modules that contain both a static memory and a battery. Dallas Semiconductor specifies the modules to retain data for five years. SGS-Thomson uses a lithium carbon monofluoride battery and predicts battery life of 11 years at 70°C. The fundamental problem

with battery-backed SRAMs is that the battery is a wasting asset. When the battery dies, your system power supply will still let you use the memory, but you might turn off your system mistakenly thinking that your data is safe.

Dallas Semiconductor protects data stored in DRAMs with its DRAM Nonvolatizer controller chip that you can purchase individually (\$7 (100)) or as part of a SIMM (single in-line memory module). You supplement the primary power supply with capacitors, a NiCd battery, or lithium batteries. The DRAM Nonvolatizer provides timing, refresh generation, and power-up and power-down sequencing to protect your data in case of system power failure. The Nonvolatizer is automatically activated when the primary supply voltage drops below 4.5V. The system retakes control when its voltage exceeds 4.5V and a software-controlled switch is set.

Although battery-backed SRAMs and DRAMs aren't truly nonvolatile memories, you can use them in certain applications providing that you can periodically check the battery's charge status and replace the battery before it runs down. And although ferroelectric RAMs are not yet made in meaningful quantities or densities, they promise to bridge the gap between volatile and nonvolatile memories.

On the other hand, there is no shortage today of true nonvolatile-memory types. If your design goals are realistic, then there's sure to be a nonvolatile memory among the ROM, PROM, OTP, EPROM, EEPROM, flash, nonvolatile SRAM, and ferrite-core chips that fits your cost, performance, and density needs.

EDN

Tables continued on pg 106

References

1. Gallant, John, "Conventional EEPROMs and flash EEPROMs offer a spectrum of bit densities," *EDN*, October 27, 1988, pg 89.
2. Lahti, Walt, "Flash Memory," *In-Stat*, April, 1989.

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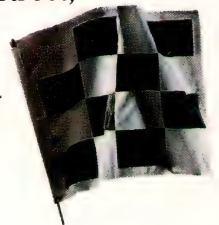
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TABLE 2—REPRESENTATIVE ROMs

PART NUMBER	SPEED	DENSITY (BITS)	ORGANIZATION	POWER (TTL)		PRICE	COMMENTS
				ACTIVE	STAND BY		
AMD 27x512	150 nSEC	512k	64kx8	50 mA	2 mA	\$4.25 (10,000)	ONE-TIME-PROGRAMMABLE VERSION IN PLASTIC. FACTORY PROGRAMMED.
GOULD/AMI S631000 S63512 S63256	150 nSEC	1M	128kx8	50 mA	2 mA	\$6.20 (10,000)	MINIMUM 1000-PIECE ORDER.
	150 nSEC	512k	64kx8	50 mA	2 mA	\$3.90 (10,000)	
	100 nSEC	256k	32kx8	40 mA	2 mA	\$2.30 (10,000)	
MICROCHIP RO9C256	250 nSEC	256k	32kx8	25 mA	3 mA	\$2.65 (10,000)	10-WEEK DELIVERY. AVAILABLE IN 150-nSEC VERSION.
SHARP LH531 LH532 LH534 LH538	250 nSEC	1M	128kx8	25 mA	2 mA	\$4.75 (100)	
	250 nSEC	2M	256kx8	35 mA	2 mA	\$8 (100)	
			126kx16				
	250 nSEC	4M	512kx8	50 mA	3 mA	\$14 (100)	
			256kx16				
TOSHIBA TC531000P TC543000P	250 nSEC	8M	1Mx8 512kx16	NA	NA	\$50 (100)	12-WEEK DELIVERY. 12-WEEK DELIVERY.
	120 nSEC	1M	128kx8	50 mA	2 mA	\$4.95 (5,000)	
	250 nSEC	4M	512kx8	40 mA	2 mA	\$15 (5,000)	

TABLE 3—REPRESENTATIVE ONE-TIME-PROGRAMMABLE (OTP) MEMORIES

PART NUMBER	SPEED	DENSITY (BITS)	ORGANIZATION	POWER (TTL)		PRICE	COMMENTS
				ACTIVE	STAND BY		
CYPRESS CY7C291A CY7C263	20 nSEC	16k	2kx8	120 mA	40 mA	\$15.55 (100)	NONREGISTERED.
	30 nSEC	64k	8kx8	120 mA	30 mA	\$34.75 (100)	NONREGISTERED.
FUJITSU MB8541	—	256 SERIAL	256x1	10 mA	20 μ A	\$1.95 (10,000)	21V PROGRAMMABLE, 64-BIT SERVICE CELLS.
TEXAS INSTRUMENTS TMS27PC256 TMS27PC512	150 nSEC	256k	32kx8	30 mA	NA	\$4.75 (100)	SNAP! PROGRAMMING ALGORITHM WRITES 256k-BIT OTP IN LESS THAN 4 SEC.
	200 nSEC	512k	64kx8	30 mA	NA	\$6.55 (100)	
TOSHIBA TC54512AF TC541000P-20	150 nSEC	512k	64kx8	30 mA	1 mA	\$5.70 (100)	8-WEEK DELIVERY.
	200 nSEC	1M	128kx8	30 mA	1 mA	\$14.60 (100)	8-WEEK DELIVERY.
WAFERSCALE WS27C010L	100 nSEC	1M	128kx8	NA	NA	\$44 (100)	

TABLE 4—REPRESENTATIVE PROMs

PART NUMBER	SPEED	DENSITY (BITS)	ORGANIZATION	POWER (TTL)		PRICE	COMMENTS
				ACTIVE	STAND BY		
RAYTHEON R29671 R29673	70 nSEC	32k	4kx8	195 mA	—	\$30 (100)	POWER SWITCHED, REMOVES POWER TO DEVICE WHEN NOT ACCESSED.
	85 nSEC	32k	4kx8	195 mA	55 mA	\$32.85 (100)	
R29651 R29653	60 nSEC	8k	2kx4	170 mA	—	\$5.70 (100)	POWER SWITCHED.
	65 nSEC	8k	2kx4	170 mA	45 mA	\$5.70 (100)	

NOTES: THE VOLUME OF AVAILABLE SUPPORT CHIPS PREVENTS INCLUSION OF ALL DEVICES.
FOR MORE INFORMATION, REFER TO THE MANUFACTURER'S PRODUCT LISTING.
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TABLE 5—REPRESENTATIVE EPROMs

PART NUMBER	SPEED	WRITE	DENSITY (BITS)	ORGANIZATION	POWER (TTL)		PRICE	COMMENTS
					ACTIVE	STAND BY		
AMD								
AM27C010	125 nSEC	1.05 mSEC	1M	128kx8	60 mA	1 mA	\$28.35 (100)	12.75V PROGRAM VOLTAGE. AVAILABLE IN OTP VERSION.
AM27C1024	125 nSEC	1.05 mSEC	1M	64kx16	60 mA	1 mA	\$29 (100)	12.75V PROGRAM VOLTAGE. AVAILABLE IN OTP VERSION.
AM27C512	120 nSEC	1.05 mSEC	512k	64kx8	50 mA	2 mA	\$9.58 (100)	12.75V PROGRAM VOLTAGE. AVAILABLE IN OTP VERSION.
AM27C64	55 nSEC	1.05 mSEC	64k	8kx8	50 mA	1 mA	\$15.03 (100)	12.75V PROGRAM VOLTAGE. AVAILABLE IN OTP VERSION.
ATMEL								
AT27C010	150 nSEC	105 μ SEC/BYTE	1M	128kx8	50 mA	3 mA	\$33.70 (100)	RAPID PROGRAM ALGORITHM.
AT27C512	120 nSEC	105 μ SEC/BYTE	512k	4x16kx8	25 mA	3 mA	\$14.10 (100)	FOUR PAGES OF 16kx8 BITS.
CATALYST								
CAT27HC256	55 nSEC	105 μ SEC	256k	32kx8	60 mA	40 mA	\$29.32 (1000)	QUICK-PULSE AND INTELLIGENT RAPID PROGRAM ALGORITHM ALSO AVAILABLE IN LOW-POWER VERSION.
CAT27C210	150 nSEC	105 μ SEC	1M	64kx16	60 mA	1 mA	\$18.51 (1000)	
CYPRESS								
CY7C251	45 nSEC	10 mSEC	128k	16kx8	120 mA	35 mA	\$67.05 (100)	NONREGISTERED.
CY7C265	40 nSEC	10 mSEC	64k	8kx8	120 mA	35 mA	\$38.05 (100)	REGISTERED.
CY7C271	35 nSEC	10 mSEC	256k	32kx8	120 mA	30 mA	\$123.50 (100)	POWER SWITCHED.
FUJITSU								
MBM27C1001	200 nSEC	0.525 mSEC	1M	128kx8	30 mA	1 mA	\$17 (100)	HAS SINGLE AND 4-BYTE PROGRAMMING MODES.
MBM27C512	200 nSEC	1.05 mSEC	512k	64kx8	30 mA	1 mA	\$7 (100)	
MBM27C256	200 nSEC	1.05 mSEC	256k	32kx8	30 mA	1 mA	\$5.25 (100)	
INTEL								
27C240	200 nSEC	105 μ SEC	4M	256kx16	50 mA	1 mA	\$140 (100)	QUICK-PULSE PROGRAM.
27C220	200 nSEC	105 μ SEC	2M	128kx16	50 mA	1 mA	\$55 (100)	QUICK-PULSE PROGRAM.
27C020	200 nSEC	105 μ SEC	2M	256kx8	30 mA	1 mA	\$49 (100)	QUICK-PULSE PROGRAM.
27C202	70 nSEC	105 μ SEC	256k	16kx16	100 mA	15 mA	\$40 (5000)	QUICK-PULSE PROGRAM.
MICROCHIP								
27C256	150 nSEC	1.05 mSEC	256k	32kx8	25 mA	3 mA	\$5.11 (1000)	10-WEEK DELIVERY. AVAILABLE IN OTP VERSION.
27HC64	70 nSEC	1.05 mSEC	64k	8kx8	90 mA	50 mA	\$12.70 (1000)	10-WEEK DELIVERY. AVAILABLE IN OTP VERSION. LOW-POWER OPTION HAS STANDBY MAX CURRENT OF 3mA. DEVICE AVAILABLE TO 45-nSEC ACCESS TIME.
TEXAS INSTRUMENTS								
TMS27C210	250 nSEC	NA	1M	64kx16	NA	NA	\$24.50 (100)	
TMS27C512	150 nSEC	NA	512k	64kx8	NA	NA	\$9.50 (100)	
TMS27C512	200 nSEC	NA	512k	64kx8	NA	NA	\$7.50 (100)	
TOSHIBA								
TC57H1024D	85 nSEC	100 μ SEC	1M	64kx16	40 mA	100 μ A	\$35 (1000)	12.75V PROGRAM VOLTAGE.
TC57512AD	150 nSEC	100 μ SEC	512k	64kx8	30 mA	100 μ A	\$12.35 (1000)	12.75V PROGRAM VOLTAGE.
TC574000D	150 nSEC	50 μ SEC	4M	512kx8	50 mA	100 μ A	\$110 (SAMPLE)	12.75V PROGRAM VOLTAGE.
WAFERSCALE								
WS27C512DM	120 nSEC	NA	512k	64kx8	NA	NA	\$29.30 (100)	MILITARY-SPEC VERSION.

TABLE 6—REPRESENTATIVE EEPROMs

PART NUMBER	SPEED	WRITE	DENSITY (BITS)	ORGANIZATION	POWER (TTL)		PRICE	COMMENTS
					ACTIVE	STAND BY		
AMD								
AM2864AE	200 nSEC	10 mSEC	64k	8kx8	140 mA	70 mA	\$14.25 (100)	DATA POLLING. SELF-TIMED WRITE CYCLE. BYTE OR PAGE WRITE.
ATMEL								
AT28C1024	120 nSEC	10 mSEC	1M	64kx16	100 mA	5 mA	\$750 (100)	PAGE WRITE. CONTROL TIMER. SOFTWARE PROTECTION.
AT28HC16L	45 nSEC	1 mSEC	16k	2kx8	80 mA	3 mA	\$16.09 (100)	DATA POLLING.
AT28PC64	150 nSEC	2 mSEC	64k	8kx8	80 mA	3 mA	\$12 (100)	

NOTES: THE VOLUME OF AVAILABLE SUPPORT CHIPS PREVENTS INCLUSION OF ALL DEVICES.
FOR MORE INFORMATION, REFER TO THE MANUFACTURER'S PRODUCT LISTING.
NA = NOT AVAILABLE

Tables continued

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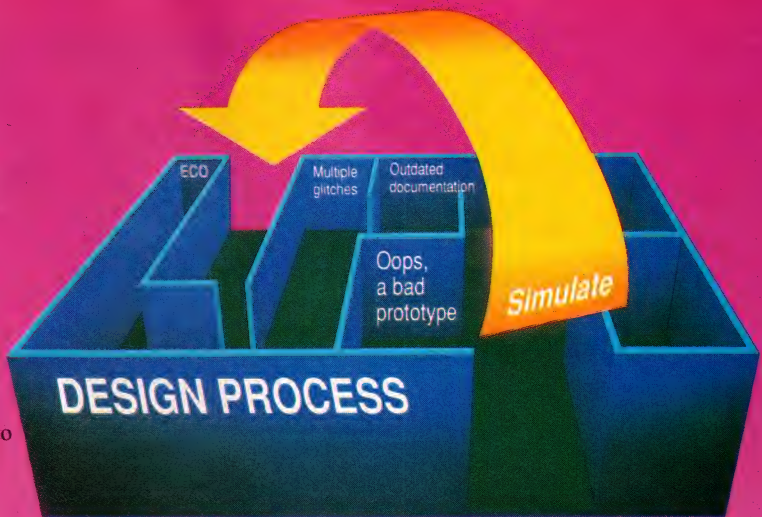
A: To save money.

If your design goes through several iterations, is the documentation still accurate? Suddenly your time and budget are being spent on laying in patches, not producing.

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Your schematic is supposed to be the best answer to someone else's design problem. Think of how great you'll look when you present a solution with no glitches, timing violations or other problems.

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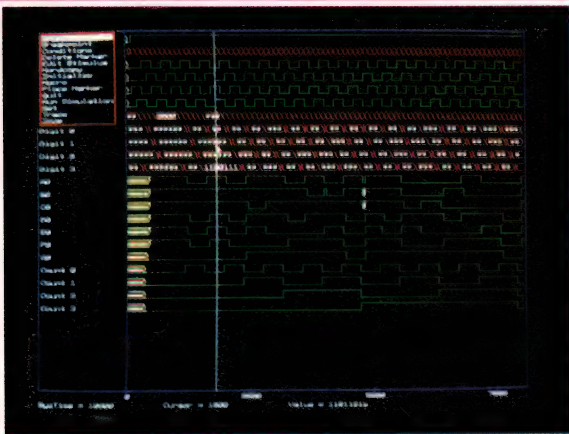
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TABLE 6—REPRESENTATIVE EEPROMs (Continued)

PART NUMBER	SPEED	WRITE	DENSITY (BITS)	ORGANIZATION	POWER (TTL)		PRICE	COMMENTS
					ACTIVE	STAND BY		
CATALYST CAT93C46P	—	10 mSEC	1k SERIAL	64x16 OR 128x8	3 mA	100 μ A	\$1.40 (1000)	AVAILABLE IN 100-YEAR RETENTION. 100,000 WRITE-CYCLE VERSION. f=700 kHz. AVAILABLE IN 3V VERSION. WRITE PROTECTION. WRITE-CYCLE TIME-OUT. f=1 MHz. f=5 MHz. FEATURES SECURE-ACCESS DEVICE WITH USER-DEFINED PASSWORD. AVAILABLE IN 3V VERSION. DATA POLLING. 10-YEAR RETENTION. 10,000 WRITE-CYCLE ENDURANCE. SELF-TIMED WRITE. DATA PROTECTION.
CAT35C102P	—	10 mSEC	2k SERIAL	128x16 OR 256x8	3 mA	100 μ A	\$2.16 (1000)	
CAT35C704	—	10 mSEC	4k SERIAL	256x16 OR 512x8	3 mA	100 μ A	\$6.50 (1000)	
CAT28C16A	200 nSEC	10 mSEC	16k	2kx8	35 mA	1 mA	\$3.09 (1000)	
EXEL XL2865A	250 nSEC	10 mSEC	64k	8kx8	110 mA	50 mA	\$12.75 (100)	10 YEAR/10k WRITE ENDURANCE. DATA POLLING. WRITE TIME-OUT. READY/BUSY STATUS PIN. ERASE/BEFORE WRITE, 5V, PAGE WRITE, FALSE WRITE PROTECTION. 10 YEAR/10k WRITE ENDURANCE, DATA POLLING, WRITE TIME-OUT, ERASE BEFORE WRITE, PAGE WRITE, FALSE WRITE PROTECTION. 5V. 10 YEAR/10k WRITE ENDURANCE. WRITE TIME-OUT, ERASE BEFORE WRITE, WRITE PROTECTION. 5V. f=250 kHz 10 YEAR/10k WRITE ENDURANCE, WRITE TIME-OUT. 5V. READY/BUSY STATUS, FALSE WRITE PROTECTION. 5V. 10.8 TO 20.5V PROGRAM VOLTAGE. BYTE WRITE AFTER CHIP RESET. FULLY STATIC 5 mSEC BYTE WRITE.
XL2864A	250 nSEC	10 mSEC	64k	8kx8	110 mA	50 mA	\$12.75 (100)	
XL2816A	250 nSEC	10 mSEC	16k	2kx8	110 mA	50 mA	\$5.27 (100)	
XL93C46	—	10 mSEC	1k SERIAL	64x16	3 mA	1 mA	\$0.36 (100)	
XL2804A	250 nSEC	10 mSEC	4k	512x8	80 mA	40 mA	\$4.93 (100)	
XL46C15	55 nSEC	5 mSEC	16k	2kx8	90 mA	45 mA	\$5.10 (100)	
ICT 93CX66	—	10 mSEC	4k SERIAL	256x16	7 mA	200 μ A	\$5 (1000)	WRITE-CYCLE TIME-OUT. READY/BUSY STATUS. WRITE PROTECTION. f=2 MHz
93CX46	—	10 mSEC	1k SERIAL	64x16	3 mA	50 μ A	\$2.10 (1000)	
MICROCHIP 24C04	—	1 mSEC/BYTE	4k	2x256x8	4.25 mA	300 μ A	\$3.77 (1000)	WRITE PROTECTION FOR UPPER 256-BYTE BLOCK. PAGE-WRITE CAPABILITY FOR 8 BYTES. FAST VERSION READS IN 150 nSEC AND WRITES IN 200 μ SEC. DATA POLLING. CHIP-CLEAR FUNCTIONS. ELECTRONIC SIGNATURE.
28C16	200 nSEC	1 mSEC	16k	2kx8	30 mA	3 mA	\$4.27 (100)	
NATIONAL NMC9306	—	30 mSEC	256 SERIAL	16x16	14 mA	5 mA	\$0.93 (100)	10-YEAR/40k WRITE CYCLES. f=250 kHz. CMOS TO 1 MHz. 10-YEAR/40k WRITE CYCLES.
NMC9346	—	12 mSEC	1k SERIAL	64x16	15 mA	5 mA	\$1.21 (100)	
NEC μ PD28C64 μ PD28C04	200 nSEC 200 nSEC	10 mSEC 10 mSEC	64k 4k	8kx8 512x8	50 mA 17 mA	1 mA 1 mA	\$12.09 \$8.45	12-WEEK LEADTIME. 12-WEEK LEADTIME.
SEEQ 28C256A	90 nSEC	10 mSEC	256k	32kx8	80 mA	2 mA	\$350 (100)	10-YEAR/10k WRITE CYCLES, DATA POLLING, TOGGLE BIT, HARDWARE AND SOFTWARE DATA PROTECTION, PAGE WRITE.

NOTES: THE VOLUME OF AVAILABLE SUPPORT CHIPS PREVENTS INCLUSION OF ALL DEVICES.
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NAME OF FIRM _____ NATURE OF BUSINESS _____

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ANNUAL SALARY \$ _____ OTHER INCOME \$ _____

SOURCE OF OTHER INCOME _____
(Alimony, child support, spousal income or separate maintenance income need not be revealed if you do not wish it considered as a basis of repayment.)

MOTHER'S MAIDEN NAME _____
(For use when you request special action on your account)

PREVIOUS FIRM _____ YEARS THERE _____
(If at current firm less than 3 years)

PREVIOUS HOME ADDRESS _____
(If at present address less than 3 years)

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My American Express® Account # is _____

I have read the entire application, agree to its terms, and certify the information is correct.

X
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Method Of Computing The Balance For Purchases	Average Daily Balance (including new purchases)
Transaction Fee For Cash Advances, And Fees For Paying Late Or Exceeding The Credit Limit	Transaction Fee For Bank and ATM Cash Advances: 2% of each Cash Advance, \$2 Minimum, \$25 Maximum Transaction Fee For Access Check Cash Advances: 1% of each Cash Advance, \$2 Minimum, \$10 Maximum Late Payment Fee: \$15; Over-the-Credit-Limit Fee: \$15

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TABLE 6—REPRESENTATIVE EEPROMs (Continued)

PART NUMBER	SPEED	WRITE	DENSITY (BITS)	ORGANIZATION	POWER (TTL)		PRICE	COMMENTS
					ACTIVE	STAND BY		
SIERRA SC22101 SC22102 SC22104	180 nSEC 180 nSEC 180 nSEC	20 mSEC 20 mSEC 20 mSEC	1k 2k 4k	128x8 256x8 512x8	15 mA 15 mA 15 mA	5 mA 5 mA 5 mA	\$5.15 (10,000) \$6.96 (10,000) \$8.26 (10,000)	5V ONLY.
SIMTEK STK28C256	70 nSEC	10 mSEC	256k	32kx8	80 mA	1.5 mA	\$295 (100)	PAGE-WRITE. INTERNAL CONTROL-TIMER. DATA POLLING. TOGGLE BIT. HARDWARE AND SOFTWARE DATA PROTECTION.
WHITE TECH WE-256K8-150	150 nSEC	3 mSEC	2M	256kx8	90 mA	2.5 mA	\$1925 (100)	PAGE-WRITE. DATA POLLING. HARDWARE AND SOFTWARE DATA PROTECTION.
WE-128K8-150	150 nSEC	3 mSEC	1M	128kx8	80 mA	1.2 mA	\$1013 (100)	
XICOR X28C010	200 nSEC	10 mSEC	1M	128kx8	80 mA	3 mA	\$995 (100)	64-BYTE PAGE. DATA POLLING. SOFTWARE DATA PROTECTION. TOGGLE BIT. MODULE ONLY. AVAILABLE IN NMOS. 64-BYTE PAGE. DATA POLLING. SOFTWARE DATA PROTECTION. TOGGLE BIT. AVAILABLE IN CMOS. 32-BYTE PAGE. DATA POLLING. 16-BYTE PAGE. DATA POLLING. 3 TO 6V OPERATION. f=100 kHz. 3 TO 6V OPERATION.
X28C256B	150 nSEC	10 mSEC	256k	32kx8	60 mA	2 mA	\$206 (100)	
X2864H	70 nSEC	5 mSEC	64k	8kx8	150 mA	80 mA	\$98 (100)	
X2816B	250 nSEC	10 mSEC	16k	2kx8	140 mA	60 mA	\$9.50 (100)	
X24C16	—	10 mSEC	16k SERIAL	2kx8	3 mA	150 μ A	\$13.86 (100)	
X24C04	—	10 mSEC	4k SERIAL	512x8	3 mA	150 μ A	\$7.34 (100)	

TABLE 7—REPRESENTATIVE FLASH MEMORIES

PART NUMBER	SPEED	WRITE	DENSITY (BITS)	ORGANIZATION	POWER (TTL)		PRICE	COMMENTS
					ACTIVE	STAND BY		
ATMEL AT29C256	150 nSEC	10 mSEC	256k	32kx8	80 mA	3 mA	\$25 (100)	ERASE AND PROGRAM IN ONE CYCLE. DATA POLLING. DATA PROTECTION. 1000 ERASE/PROGRAM. 10-YEAR, 5V PROGRAM.
INTEL 28F010	120 nSEC	120 nSEC	1M	128kx8	30 mA	1 mA	\$38 (10,000)	12V PROGRAM VOLTAGE. 10,000 ERASE AND PROGRAM CYCLES. 12V PROGRAM VOLTAGE. 10,000 ERASE AND PROGRAM CYCLES.
28F512	120 nSEC	120 nSEC	512k	64kx8	30 mA	1 mA	\$21 (10,000)	
SEEQ 48F010	250 nSEC	150 μ SEC	1M	128kx8	60 mA	5 mA	\$93.75 (100)	100 WRITE-CYCLE ENDURANCE. 10-YEAR RETENTION. 12.75V PROGRAM VOLTAGE. SECTOR ERASE.
48F512	250 nSEC	150 μ SEC	512k	64kx8	60 mA	5 mA	\$34.90 (100)	
TOSHIBA TC58257	200 nSEC	1.05 mSEC	256k	32kx8	30 mA	1 mA	\$15 (100)	100 WRITE-CYCLE ENDURANCE. 100- μ SEC WRITE PULSE. 12.75V PROGRAM VOLTAGE.

Tables continued

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Add a **Ripple Attenuator Module™** to any Vicor VI-200™ converter, MegaModule™, MasterModule™ or FlatPAC™ with output voltages from 5 to 50 Volts and limit total output noise to less than **2mV, peak-to-peak** at loads up to 10 Amps. Combining active and passive filtering, RAMs attenuate both low frequency line harmonics and high frequency switching components in the range of DC to 20 MHz...by approximately 40 dB. No adjustments are required, and remote sense and output voltage trim features are retained.

RAMs Are Available In Three Product Grades:

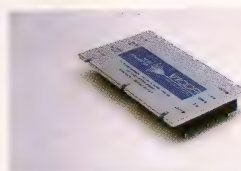
■ Commercial	0°C to +85°C	VI-RAM-C1
■ Industrial	-40°C to +85°C	VI-RAM-I1
■ Military	-55°C to +100°C	VI-RAM-M1

VI-RAM™
Ripple Attenuator Module
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2 mV/cm

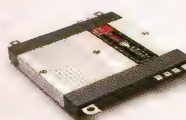
VI-RAMs Are Designed For Use With The Following Products:

VI-200™ Series DC-DC Converters and Power Boosters™



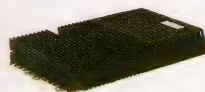
- 12 to 300 VDC nom. inputs
- Single output, 2-95 Volts
- 50, 75, 100, 150, 200 Watts
- Up to 36 Watts/cubic inch
- UL, CSA, TUV

Mega/Master Module™ Series High Power DC-DC Converters



- 12 to 300 VDC nom. inputs
- Single, dual and triple output
- Up to 600 Watts
- Up to 27 Watts/cubic inch
- UL, CSA, TUV

FlatPAC™ Series High Power AC-DC Switchers



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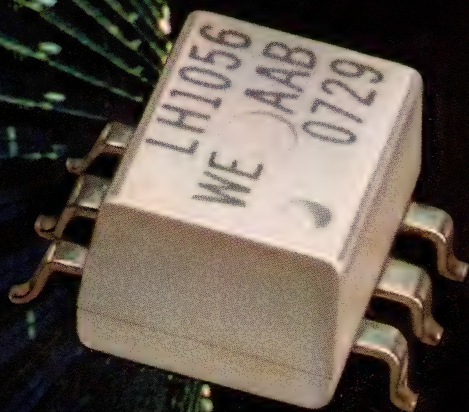
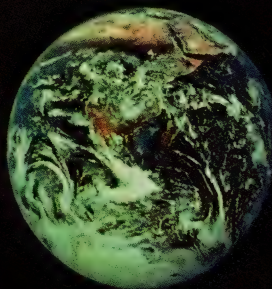
TABLE 8—OTHER REPRESENTATIVE NONVOLATILE MEMORIES

TYPE	PART NUMBER	SPEED	WRITE	DENSITY (BITS)	ORGANIZATION	POWER (TTL)		PRICE	COMMENTS
						ACTIVE	STAND BY		
CORE	CONTROLEX 125	2.5 μ SEC	7 μ SEC	8	1x8			\$20 (100)	DRIVE CURRENT: 350-mA READ, 40-mA WRITE. 0–50°C TEMPERATURE RANGE. READ IS DESTRUCTIVE. DRIVE CURRENT: 400-mA CLEAR, 200-mA READ, 50-mA WRITE. MILITARY TEMPERATURE RANGE NONDESTRUCTIVE READ RADIATION HARD. DRIVE CURRENT: 350-mA READ AND WRITE. 0–200°C OPERATING RANGE. DRIVE CURRENT: 80-mA SET AND RESET.
	126	500 nSEC	10 μ SEC	4	1x4			\$125 (100)	
	128	1 μ SEC	1 μ SEC	512	64x8			\$150 (100)	
	120	2 μ SEC	2 μ SEC	4 SERIAL	1x4			\$7 (100)	
DRAM	DALLAS SEMI- CONDUCTOR DS2219	120 nSEC	120 nSEC	1M +PARITY	1kx9	15 mA PLUS HITACHI HB56A19B		\$228 (100)	CONTROLLED BY DS1237 7/100. DRAM SIMM MODULE CAPACITORS. NiCd BATTER- IES OR LITHIUM BATTERIES PROVIDE BACK-UP POWER.
FERRO- ELECTRIC RAM	KRYSALIS K74CF372	3.3 mSEC	3.3 mSEC	8	8x1	12 mA	1.3 mA	\$8.50 (100)	10 ¹¹ WRITES 1 YEAR BE- TWEEN USE.
SRAM	DALLAS SEMI- CONDUCTOR DS1245	70 nSEC	70 nSEC	1M	128kx8	85 mA	10 mA	\$199 (100)	EMBEDDED LITHIUM BAT- TERY. MIN 5-YEAR RETENTION. EMBEDDED LITHIUM BAT- TERY. 11-YEAR RETENTION AT 70°C.
	SGS-THOMSON MK48Z08	150 nSEC	150 nSEC	64k	8kx8	50 mA	3 mA	\$15 (1000)	
NON- VOLATILE RAM	CATALYST CAT22C10	200 nSEC/ 1400 nSEC	200 nSEC/ 10 mSEC	256	64x4	40 mA	30 μ A	\$5 (1000)	10-YEAR RETENTION/ 10,000-WRITE ENDURANCE. f=1 MHz
	CAT22C12	200 nSEC/ 1400 nSEC	200 nSEC/ 10 mSEC	1k	256x4	50 mA	30 μ A	\$7 (1000)	
	CAT24C44	-/2500 nSEC	200 nSEC/ 10 mSEC	256 SERIAL	16x16	20 mA	30 μ A	\$2.25 (1000)	
	SIMTEK STK10C68A	35 nSEC/ 40 μ SEC	35 nSEC/ 10 mSEC	64k	8kx8	90 mA	2 mA	\$48.75 (100)	HARDWARE SEQUENCE TRANSFER FROM SRAM TO EEPROM OR BACK. SOFTWARE SEQUENCE TRANSFER FROM SRAM TO EEPROM OR BACK. 10 ⁵ EN- DURANCE. RECALL ON PULSE-UP.
	STK11C68A	35 nSEC/ 40 μ SEC	35 nSEC/ 10 mSEC	64k	8kx8	90 mA	2 mA	\$48.75 (100)	
	XICOR X2201	300 nSEC/ 1200 nSEC	300 nSEC/ 10 mSEC	1k	1kx1	60 mA	—	\$15.20 (100)	
	X2212	300 nSEC/ 1200 nSEC	300 nSEC/ 10 mSEC	1k	256x4	70 mA	—	\$10.89 (100)	
	X2001	200 nSEC/ 5 μ SEC	200 nSEC/ 10 mSEC	1k	128x8	100 mA	65 mA	\$11.70 (100)	
	X2210	300 nSEC/ 1200 nSEC	300 nSEC/ 10 mSEC	256	64x4	55 mA	—	\$5.59 (100)	
	X2004	200 nSEC/ 5 μ SEC	200 nSEC/ 10 mSEC	4k	256x8	120 mA	90 mA	\$23.15 (100)	

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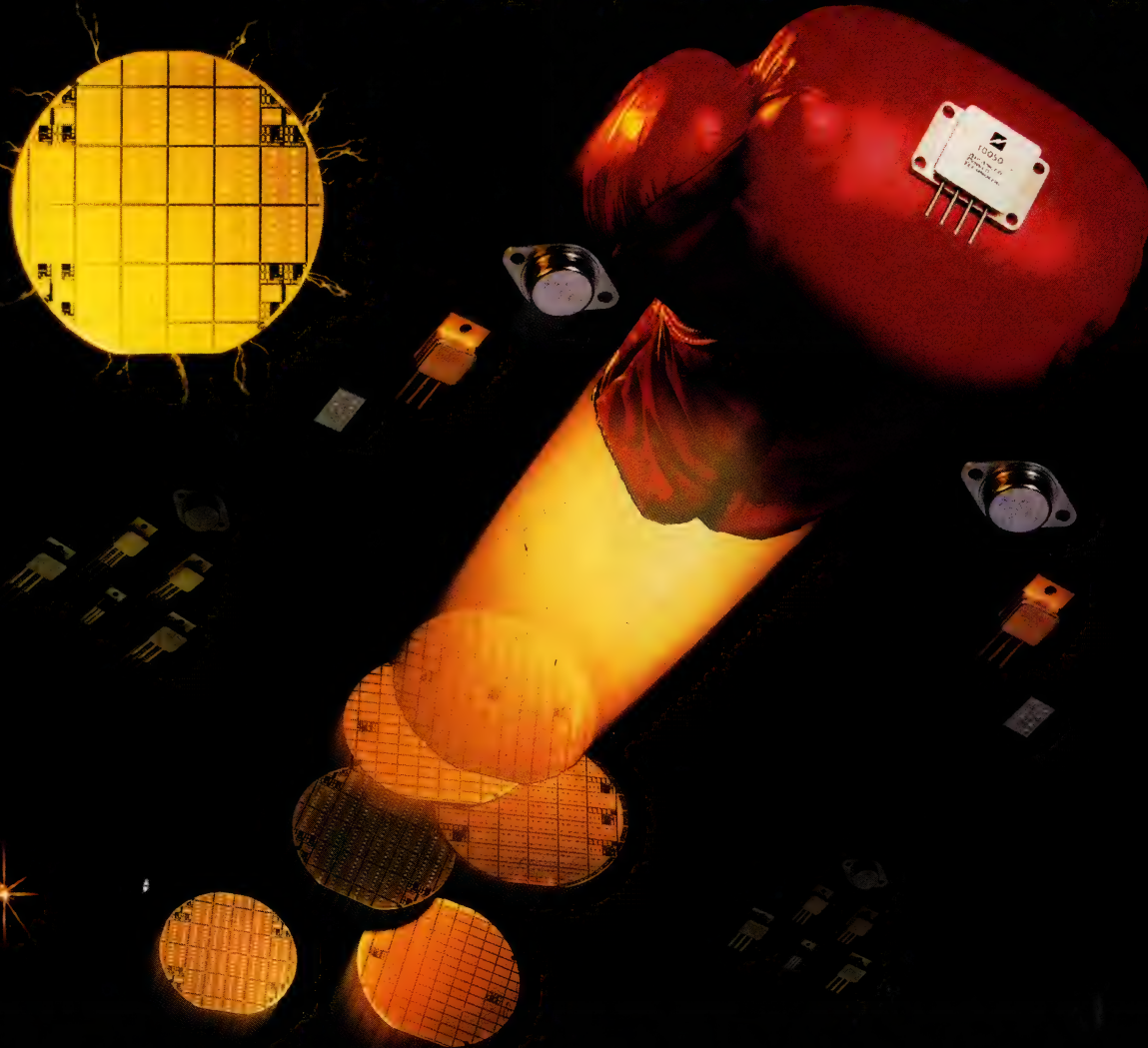
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R _{DS(ON)} - Ω From - To	I _D - Amps From - To	I _{DM} - Amps From - To	C _{iss} - pF Min. - Max.	Q _g - nC Min. - Max.	Die Size Inches (No.)
0.021 - 0.21	95.0 - 39.0	380 - 156	9000 - 13000	360 - 675	0.738 × 0.585 (108)
0.04 - 0.40	83.0 - 20.5	332 - 82	4500 - 6500	160 - 370	0.588 × 0.388 (107)
0.20 - 1.30	26.0 - 8.5	104 - 34	1800 - 2950	60 - 130	0.414 × 0.254 (106)
0.30 - 2.40	18.5 - 5.0	74 - 20	1300 - 1800	45 - 105	0.290 × 0.250 (105)
0.65 - 4.20	11.0 - 3.0	44 - 12	650 - 950	20 - 55	0.199 × 0.203 (104)

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Proper output decoupling maximizes power-supply operation

The decoupling technique presented here lets you develop an optimum supply-load decoupling network. You need to know only two values—the supply's output impedance and the capacitor's impedance characteristics—to solve noise problems without causing oscillation.

Steven C Hageman, *Calex Mfg Co Inc*

When you're decoupling a power supply, your goal is to reduce the supply's high-frequency impedance without turning the supply into a giant power oscillator. To reduce power-supply noise, don't just grab the highest value, lowest impedance capacitor you can find, connect it across the supply output, and assume that you've solved noise problems. This hit-or-miss approach can cause more problems than it solves. Power-supply noise problems aren't caused by the power supply alone—load interactions and switching transients contribute significantly to the amount of noise. The following decoupling technique solves all of these problems and works for all supplies—switching or linear, discrete or monolithic—regardless of output-power level. To use this technique, you need only two simple measurements—the supply's output impedance and the capacitor's impedance characteristics.

The basic block diagram is pretty much the same for both linear and switching power supplies. A difference amplifier senses the supply output and compares it to a reference voltage. The output of the amplifier drives a modulator in a manner that produces a -180° phase shift throughout the system at dc. This type of negative feedback electronically reduces the supply's output impedance to make load regulation figures much better than they are for an open-loop system.

You'd expect a basic power supply to have a low output impedance (good load regulation) for all frequencies. However, power-supply designers have to roll off the gain of the feedback amplifiers as the frequency increases, so the supply's output impedance increases as the frequency increases. In other words, the output impedance is actually inductive for some frequency ranges.

Fig 1a shows how this frequency-dependent impedance characteristic develops. As shown, a 10Ω resistive source serves to model the modulator—real power supplies may have resistance values ranging from hundreds of milliohms to hundreds of ohms. Fig 1a includes an op amp with a 60-dB open-loop gain that's configured as an inverting integrator to model the error amplifier. The loop gain of the error amplifier reduces the output impedance of the Z_M as this equation shows:

$$Z_{OUT} = Z_M / (1 + T), \quad (1)$$

where T equals the overall loop gain.

At dc, the system's loop gain equals the 60-dB open-

All capacitors have at least two parasitic elements—equivalent series resistance (ESR) and equivalent series inductance (ESL).

loop gain of the op amp minus the 6-dB loss of the 2:1 voltage-sensing divider, or 54 dB. At dc, Eq 1 yields an output impedance of $10\Omega/502$, or 19.9 m Ω . At high frequencies, the loop gain is zero and the output impedance is $10\Omega/1+0$, or 10 Ω . Between these frequencies, the output impedance increases, starting at 35 Hz (because of the integrator pole) with a slope of +1—that is, a $10\times$ increase in frequency will cause a $10\times$ increase in the supply's output impedance (Fig 1b).

Unfortunately, you can't use a simple resistor to model the open-loop impedance of all power supplies. The output also contains capacitors, and, in the case of switching supplies, inductors. Because feedback theory forces designers to close the feedback loop at a single-pole rate, the output impedance always approximates the curve shown in Fig 1b, deviating slightly at very low or very high frequencies.

Fig 1c shows a linear equivalent circuit for the output impedance of the regulator of Fig 1a. By plotting the output impedance on reactance paper (see box, "Determine output impedance"), you can readily derive the circuit values. You can then read the values for R_{DC} , R_{HF} , and L directly from the graph. The equivalent circuit of Fig 1c will suffice for almost all regulators.

Consider dynamic load interactions

A power supply reacts to any load demand by presenting an output impedance that matches the output impedance of the load at the load's fundamental excitation frequency. For a dc load, this impedance equals 20 m Ω . If the supply is driving a load such as an oscillator that draws a 10-mA sine-wave current at 2000 Hz, the supply's output impedance would be 1.2 Ω , and a 12-mV sine wave would ride on the output of the power supply. At any frequency over 20 kHz, the supply's output impedance equals 10 Ω .

Supplies also have to drive step-type loads quite often. The equivalent frequency for step loads equals $0.35/(\text{rise time})$. If you were to impress a 100-mA step load with a rise time of 1 μsec on the power supply, the power supply's output would present an impedance of 10 Ω . (The equivalent frequency of the step is 350 kHz.)

Proper decoupling improves supply response

Fig 2a shows the results of adding a 47- μF capacitor to the output of the supply in Fig 1a. This illustration shows the supply's response before and after the addition of the capacitor. The capacitor reduces the peak

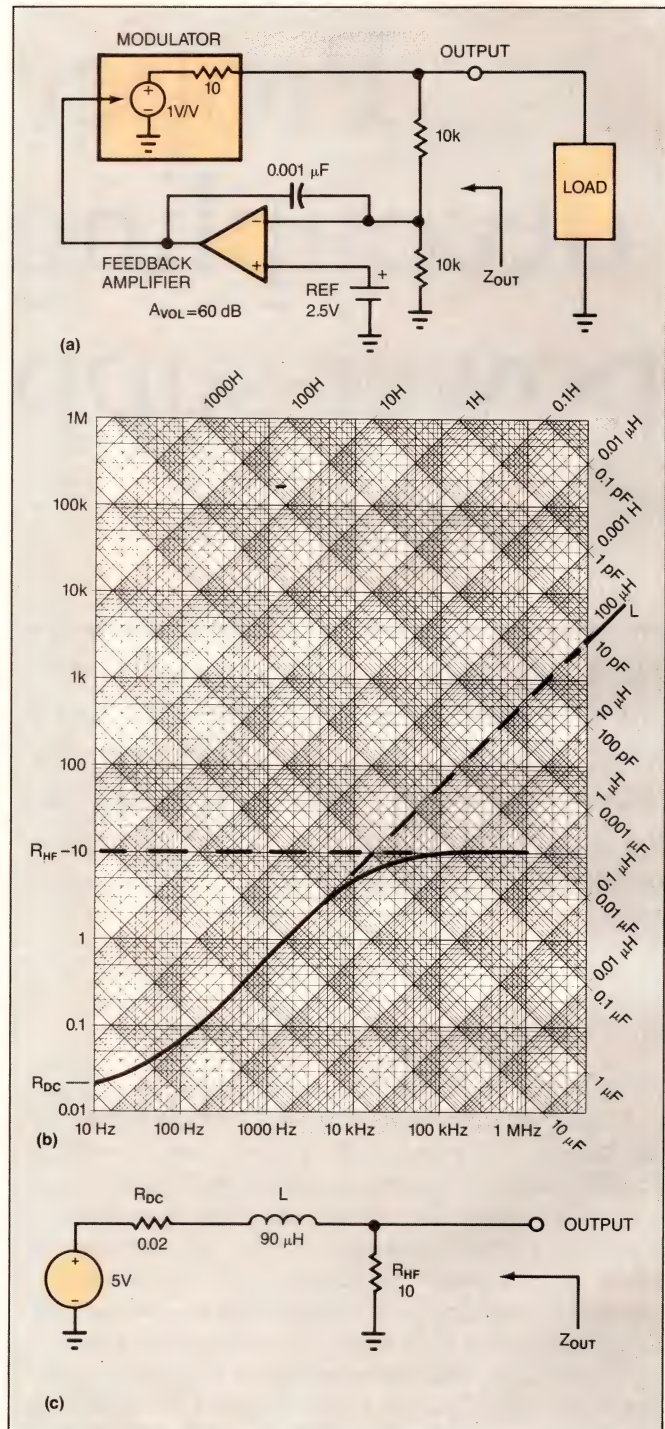


Fig 1—You can model all power supplies in a similar manner. At low frequencies, overall loop gain is a function of amplifier loop gain (a). As the frequency increases, the supply's output impedance increases in a linear fashion (b) until it flattens in the 100-kHz range. You can develop a linear equivalent circuit (c) to plot the supply's output versus frequency characteristics.

voltage, but introduces a 2.5-kHz oscillation on the output. In essence, the 47- μ F capacitor brings the power supply to the brink of sustained oscillation. Fig 2b shows why this problem occurs. When you overlay the impedance of a 47- μ F capacitor on the power supply's output impedance, the two impedance curves intersect at 2.5 kHz, causing oscillation.

The intersection occurs at a rate-of-slope-change of 2 (the increasing slope of the inductor plus the decreasing slope of the capacitor). At a given frequency, any rate-of-slope-change greater than 1 adds significant phase shift to the power supply's feedback loop. This phase shift makes the supply potentially unstable and violates the fundamental rule that Bode developed for feedback stability. At the 2.5-kHz crossover, the combined circuit forms an LC (inductance/capacitance) tank, and the output impedance actually has a peak value of 10 Ω at 2.5 kHz.

Actually, it's impossible to find a perfect 47- μ F capacitor. All real capacitors have at least two parasitic elements—equivalent series resistance (ESR) and equivalent series inductance (ESL) (see box, "Know

your capacitors"). For a 47- μ F, subminiature, aluminum electrolytic capacitor, the ESR might be in the 2 to 5 Ω range. Such values will flatten the capacitor's impedance curve well before it intersects with the supply's output impedance curve, eliminating the possibility of severe impedance peak. For a high-quality tantalum capacitor, the ESR might be in the 0.1 to 0.3 Ω range, and the response and ringing shown in Fig 2b will definitely occur. The hit-or-miss approach to power-supply decoupling causes problems because of parasitic elements such as these. Proper decoupling depends more on the construction and type of capacitor than on its value.

Figure it out, don't guess

Once you've used the known system load transients to establish the maximum desired impedance at the frequency or frequencies in question, you should check to see that the power supply itself meets your design requirements. Most well-designed, commercial power supplies provide sufficiently low output impedance to satisfy 99% of all applications. However, if you need

Determine output impedance

You can easily measure a power supply's output impedance using the circuit shown in Fig A. The function generator introduces a small ac current into the output

of the power supply. This current produces a voltage at the power-supply output that's directly proportional to the output impedance at that frequency.

By varying the frequency of the function generator in a 1-2-5 sequence over a range of 10 Hz to 1 MHz, you can generate an accurate plot of output impedance versus frequency. To take worst-case effects into consideration, you should repeat the plot at the high- and low-input line voltages and for the highest and lowest expected loads. You should then repeat the plot at the highest and lowest expected operating temperatures for these two worst-case combinations.

By plotting the output impedance on reactance paper, you can develop a linear equivalent circuit of the power supply. You can then read the values for R_{DC} , R_{HF} , and L directly from the graph.

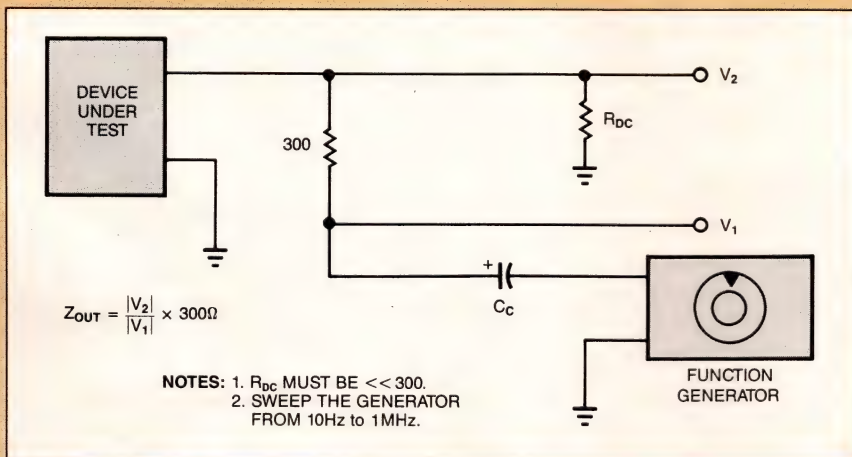


Fig A—You can accurately plot output impedance by varying the frequency of the function generator in a 1-2-5 sequence over 10 Hz to 1 MHz.

On occasion, it will be impossible to use a single-section damping network to achieve your design goal.

to improve your supply-load combination, you can take the following design steps to improve the output-impedance characteristics of the power supply.

- Determine the power supply's output impedance curve.
- Calculate the maximum desired output impedance over the pertinent range of frequencies for your load.
- Determine which decoupling network (Fig 3) will provide the desired output impedance.
- Calculate the component values for the damping network.
- After you add the damping network, verify the output impedance to see if any resonant peaks are present.

In Fig 3a, the power-supply output features a single RC decoupling network. You might need to use a discrete resistor for R_D in some cases; in other instances, the capacitor's ESR can serve as R_D . This RC network is designed to provide a high-frequency impedance of

R_D to the load. You can choose the capacitance value by using the equation

$$C = 1/2\pi f R_D \quad (2)$$

You have to select the break frequency (f) so that the break occurs somewhere below the intersection of the capacitor impedance and the output impedance of the supply. To minimize peaking, select a break frequency that occurs anywhere from 0.1 to 0.7 of the non- R_D crossing frequency. To ensure that the damping circuit will exhibit a critically damped (or overdamped) characteristic, choose a break frequency of less than 0.4.

For real-world components, size and ESR limitations may make it impossible to attain the desired output impedance with a single RC decoupling network. The dual-decoupling-network design shown in Fig 3b solves such problems. C_1 and R_{D1} allow you to flatten the supply's output impedance at a low frequency; you can

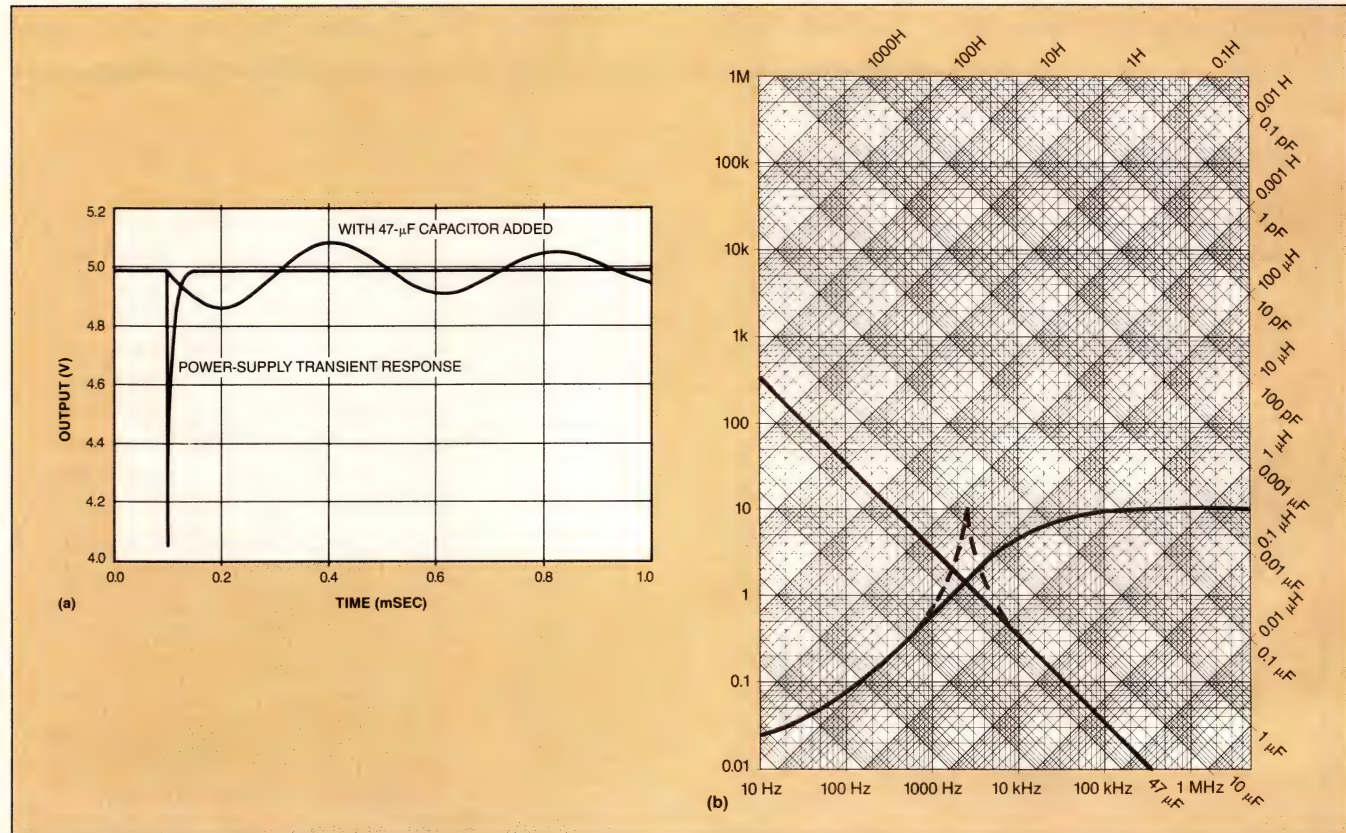


Fig 2—You'll almost certainly increase noise problems by taking a hit-or-miss approach to decoupling. You can reduce peak noise voltage by indiscriminately adding a high-value capacitor to the supply output, but this method introduces oscillation (a). This approach also violates the fundamental rules of feedback theory and develops a significant output-impedance spike (b).

Know your capacitors

Like all electronic parts, capacitors have parasitic components that cause them to deviate from their ideal characteristics. For capacitors, equivalent series resistance (ESR) and equivalent series inductance (ESL) are the most important parasitics in power-supply design.

These parasitic elements aren't constant with time, temperature, or frequency. ESR may be as much as ten times higher at 100 Hz than at 100 kHz. Thus, when most power-supply designers talk about ESR, they're really talking about the maximum capacitor impedance in the flattened portion of the impedance curve.

ESR also varies from unit to unit and with temperature. Unit-to-unit ESR variation for capacitors that have no impedance specification can be 5:1 or greater; 2:1 ESR variations are common for capacitors that have ESR characterizations. In temperature, ESR may vary by as much as 100:1 over -55 to $+105^{\circ}\text{C}$. Most of the ESR variation (30:1 change) occurs between $+25$ and -50°C .

For most well-designed capacitors, ESL has no effect on impedance until beyond 1 MHz. However, certain aluminum electrolytic capacitors have an ESL as high as $1\ \mu\text{H}$, and this high value can indeed change the impedance-versus-frequency picture. Manufacturers rarely specify ESL; it's a construction- or lead-length problem that typically results in a 4:1 maximum ESL variation with temperature or from unit to unit.

ESR and ESL also change with time; the older the capacitor and the hotter it's been running, the higher the ESR and ESL. Electrolytic drying-out effects are the culprit here. Over the useful life of a capacitor, 4:1 changes in impedance are not unusual at 100 kHz.

Power-supply designers typically use three types of capacitors—aluminum electrolytic, tantalum electrolytic, and ceramic. Each has its own unique advantages and disadvantages.

Aluminum electrolytics have capacitance values from $0.1\ \mu\text{F}$ to at least $20,000\ \mu\text{F}$. Not all manufacturers specify the maximum impedance of their aluminum capacitors or specify how impedance changes over temperature. It's safe to assume, however, that a capacitor with an impedance specification will have better ESR and ESL tolerances.

In power-supply work, you should always use an aluminum capacitor rated to operate at 105°C to improve circuit reliability. These devices have a high capacitance per unit volume and a good $C \times \text{ESL}$ product. To maximize reliability, you should derate all capacitor specifications. Aluminum capacitors are used extensively in power-supply designs and have excellent lifetimes when they are properly derated.

Tantalum capacitance values range from 0.1 to $680\ \mu\text{F}$. Tantalum capacitors are the best choice for circuits where you need a small-size unit with low impedance values.

As with aluminum electrolytic capacitors, not all tantalum-capacitor vendors specify the maximum impedance. ESR variation with temperature or from unit to unit is approximately the same for both aluminum and tantalum capacitors; tantalum units have better temperature stability, however. They also have very high capacitance per unit volume and an excellent $C \times \text{ESR}$ product. Tantalum capacitors are smaller than comparable aluminum capacitors, so they have a lower ESL.

In most cases, tantalum capacitors provide excellent bypassing performance over a wide tem-

perature range. Again, for highest reliability, you should significantly derate capacitor specifications.

Ceramic capacitors are available with values ranging from tens of picofarads to tens of microfarads, and they provide excellent high-frequency bypassing at frequencies to 50 MHz. Several dielectrics are available with different temperature characteristics and stabilities. Capacitance values of 0.01 to $1\ \mu\text{F}$ are most commonly used in power supplies. Typically, ceramic capacitors have very low ESR values, and ESL and wire lead length dominate capacitor impedance at high frequencies.

Self-resonant frequency is a term associated with ceramic capacitors. At this frequency, a ceramic capacitor resonates with its own inductance like an LC tank does. The self-resonant frequency of a ceramic capacitor is usually in the 2- to 50-MHz range. Self-resonant frequency is inversely proportional to the size of the capacitor—the larger the capacitor, the lower the frequency. Ceramic capacitors have a low capacitance value per unit volume and a very high $C \times \text{ESR}$ product. To lengthen the life of a ceramic capacitor, you should derate voltage ratings by at least 40%.

When selecting capacitors for your power-supply designs, it's best to make all your own measurements. This is the step where a very good LCR meter or low-frequency network analyzer pays for itself. Your primary concerns should be temperature, unit-to-unit parameter variations, and long-term changes in the capacitor's characteristics. The power supply isn't the place to save pennies on capacitors; if the power supply fails, the entire system shuts down. Buy from vendors who offer the highest quality.

The older the capacitor and the hotter it's been running, the higher the ESR and ESL.

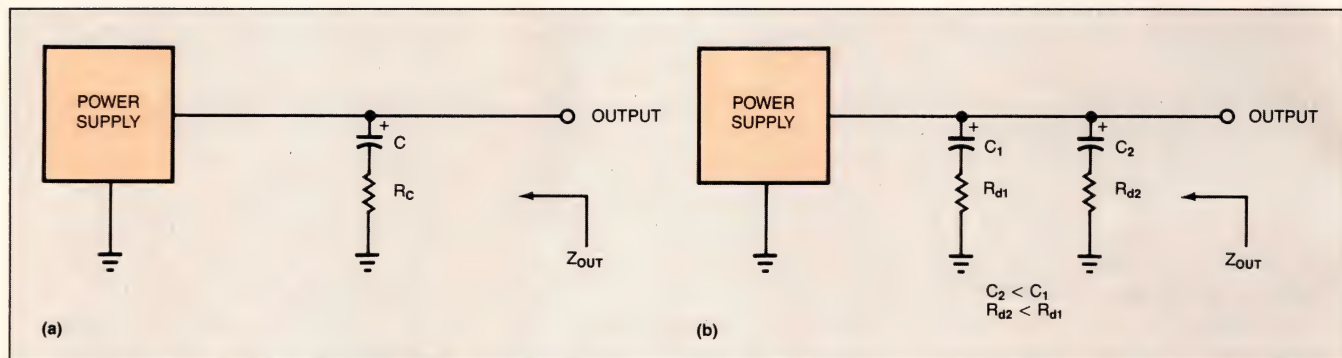


Fig 3—When your decoupling needs aren't too stringent, you can usually solve the problem with a single RC network (a). When you're dealing with real-world component limitations, a dual RC network (b) can provide the necessary decoupling performance.

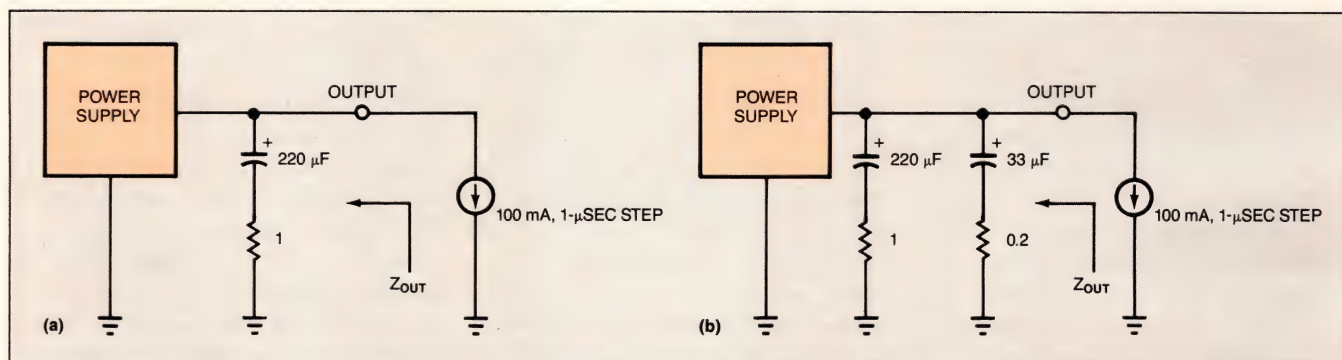


Fig 4—As long as low-frequency damping isn't a problem, you can use a single RC network (a) to decouple your power supply. When you have to worry about frequencies as low as 10 Hz, however, a dual RC network (b) may be the only way to solve decoupling problems.

then use higher-quality components for C_2 and R_{D2} to reduce the high-frequency power-supply impedance.

All circuit impedances should be at least $10\times$ higher than the impedance of the decoupling-network elements. If that's not the case, the two elements will interact. This interaction can compromise the accuracy of the damping equations. The load also acts as a damping element to further improve the decoupling network performance.

Putting theory into practice

The following examples show you how you can use the decoupling technique in the design process. First, suppose your task is to reduce the power supply's output impedance to less than 1Ω for frequencies above 1 kHz. Begin by plotting the power supply's output impedance on reactance paper. Add the desired 1Ω horizontal line to the graph. The crossing frequency will occur at 1.7 kHz. For the given conditions, choose a break frequency of 0.4 Hz (1.7 kHz) or 700 Hz. A standard 220- μF capacitor has a 700-Hz break frequency with 1Ω impedance. The resulting damping net-

work appears in Fig 4a.

When selecting the capacitor, remember that capacitor ESR is part of R_D . The capacitor shown in Fig 4a is an aluminum electrolytic unit that has an ESR of 0.2Ω . The actual discrete-resistor value shown for R_D is 0.8Ω . Use a film- or composition-type resistor rather than a wirewound unit.

On occasion, you'll find that unrealistic capacitance and ESR values make it impossible to use a single-section damping network to achieve your design goals. In these cases, you can go with a dual-damping-network scheme.

If you want to make the supply's output impedance as low as possible for frequencies above 10 Hz, 1Ω starts to look like a pretty large number. A second damping network can solve this problem, though. The design of the second damping network parallels that of the first network. The second damping capacitor's reactance should equal 1Ω at a minimum of 2.5 (that is, $1/0.4$) times the original crossing frequency. At 4250 Hz, a 33- μF capacitor has a reactance of 1.1Ω . You'd usually use a tantalum or ceramic capacitor for C_2 ,

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because these types typically have lower ESR and ESL values. C_2 's ESR can then serve as the network damping resistor. It's easy to find a 33- μ F tantalum capacitor that has an ESR of 0.2 Ω . Fig 4b shows the resulting circuit.

It's important to keep the ESL value of C_1 low at 4250 Hz to ensure that R_{d1} controls C_1 's impedance. If C_1 's ESL value controls the capacitor impedance, you'll form a secondary LC tank circuit. With high-quality impedance-specified capacitors, however, it's not a major problem.

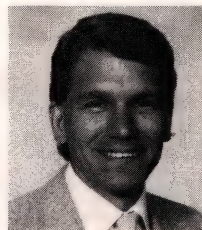
Although damping networks can substantially reduce peak overshoot, damping also increases the supply's settling time to a 1 or 0.1% error band. This settling-time increase, however, isn't as big a problem as peak overshoot values. Large peak overshoots can cause false triggering problems with flip-flops, generate glitches in digital systems, and ring through the power-supply rails of linear circuits. In the design examples, the settling time to 5 or 10% isn't a problem, because the output never exceeds the error-band level.

If you use this decoupling technique for your power supply, you'll reduce the amount of noise—without causing more problems—and increase your supply's long-term performance.

EDN

Author's biography

Steven C Hageman is the chief engineer at Callex Manufacturing Co Inc (Pleasant Hill, CA). Steve has been at Callex for five years and heads up the company's analog-design efforts for instrumentation and dc/dc converters. He holds a BSEE from the University of Santa Clara. In his spare time, Steve enjoys bicycling and PC-based analog-circuit design.

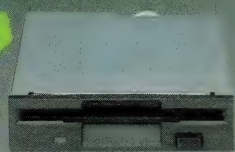


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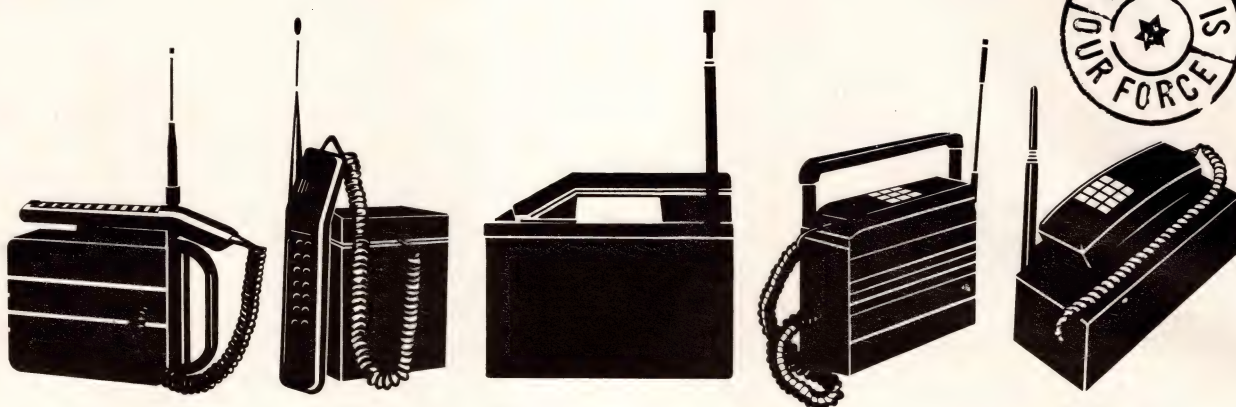
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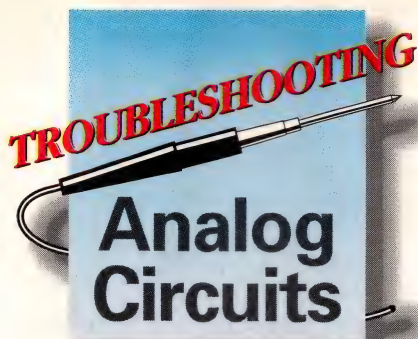
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PART 8

Keep a broad outlook when troubleshooting op-amp circuits

External components often determine an op amp's performance—that's why Bob spent the previous seven parts of this series discussing them. But op amps aren't trouble-free: Oscillations and noise are two common problems. You'll have similar trouble with buffers and comparators, which Bob will discuss in part nine.

Robert A Pease, *National Semiconductor Corp*

After many pages of fiddling around with many different components, we finally arrive at the operational amplifier itself. And the good news is that half of our problems are already solved. Why? Because it's the components around op amps that cause many of their problems. After all, the op amp is popular because external components define its gain and transfer characteristics.

So, if an amplifier's gain is wrong, you quickly learn that you should check the resistor tolerances, not the op amp. If you have an ac amplifier or filter or integrator whose response is wrong, you check the capacitor, not the op amp. If you see an oscillation, you check to see if there's an oscillation on the power-supply bus or an excessive amount of phase shift in the feedback circuit. If the step response looks lousy, you check your scope or your probes or your signal generator because they're as likely to have gone flaky as the op amp is. These failures are the reason we studied so

many passive components: The over-all performance of your circuit is often determined by those passive components. And yet, there are exceptions. There are quite a few ways an op amp itself can goof up.

Don't sweat the small stuff

Before we discuss serious problems, however, you should be aware of the kinds of op-amp errors that aren't significant. First of all, it generally isn't reasonable to expect an op amp to be linear, nor is its non-linearity all that significant. For example, what if an op amp's gain is 600,000 for positive signals but 900,000 for negative signals? This mismatch of gain slope causes a nonlinearity of about 10 μV in a 20V p-p unity-gain inverter. Heck, the voltage coefficients and temperature-coefficient errors of the feedback resistors will cause a lot more error than that! Even the best film resistors have a voltage coefficient of 0.1 ppm/V, which will cause more nonlinearity than this gain error.

Similarly, an op amp may have an offset-voltage temperature-coefficient specification of 1 $\mu\text{V}/^\circ\text{C}$, but the op amp's drift may actually be 0.33 $\mu\text{V}/^\circ\text{C}$ at some temperatures and 1.2 $\mu\text{V}/^\circ\text{C}$ at others. Twenty or thirty years ago, battles and wars were fought over this kind of specsmanship, but these days, most engineers agree that you don't need to sweat the small stuff. Most applications don't require an offset drift less than 0.99 μV for each and every degree. Most cases are quite happy when a 1 $\mu\text{V}/^\circ\text{C}$ op amp drifts less than 50 μV over 50 degrees.

When it comes to op amps, don't sweat the small stuff.

Also, you don't often need to worry about bias current and its temperature coefficient or the gain error. If the errors are well behaved and fit inside a small box, well, that's a pretty good part.

A good example of misconstrued specs is the common-mode error. We often speak of an op amp as having a CMRR of 100 dB. Does this number mean that the common-mode error is exactly one part in 100,000 and has a nice linear error of 10 μV per volt? Well, this performance is possible, but not likely. It's more likely that the offset-voltage error as a function of common-mode voltage is nonlinear (Fig 1).

It really bugs me when people say, "The op amp has a common-mode gain, A_{VC} , and a differential gain, A_{VD} , and the CMRR is the ratio of the two." This statement is silly business. It's NOT reasonable to say that the op amp has a differential gain or common-mode gain that can be represented by a single number. Neither of these gain numbers could ever be observed or measured with any precision or repeatability. Avoid the absurdity of trying to measure a "common-mode gain of zero" to compute that your CMRR slope is infinity. You'll get more meaningful results if you just measure the change in offset voltage, V_{OS} , as a function of common-mode voltage, V_{CM} , and observe the nonlinear parts of the curve. What's a good way to measure the change in V_{OS} versus V_{CM} —the CMRR—of an op amp? I know of two test circuits that work pretty well—send me your request and I'll mail you a copy. But watch out for tests that add the common-mode error and the gain error because the gain error normally overshadows the common-mode error.

Some data sheets include a CMRR-versus-frequency curve that looks the same as the gain-bandwidth-product curve, which is normally the sign of a foolish measurement error. Yes, in 1989 you can still see this kind of ridiculous curve in the data sheets of various manufacturers. The LF401's data sheet is one example, but this situation is being fixed. In most cases, you can expect an op amp's CMRR at 1 kHz to be much better than its gain at 1 kHz. If the data sheet says they're the same, then it's probably wrong.

Measure bias current rather than impedance

Another op-amp spec you don't need to worry about is the differential input impedance. Every year I still get asked, "How do we measure the input impedance of an op amp?" And every year I trot out the same answer: "We don't." Instead, we measure the bias current. There's a close correlation between the bias current and the input impedance, so if the bias current is low, the input impedance (differential and common-mode) must be high. So, let's not even think about how to measure input impedance because I haven't measured it in the last five years.

Generally, an ordinary differential bipolar stage has a differential input impedance of $1/(20 \times I_B)$, where I_B is the bias current. But this number varies if the op amp includes emitter-degeneration resistors or internal bias-compensation circuitry. You can easily test the common-mode input resistance by measuring ΔI_B versus V_{CM} .

I've measured some input capacitances and find the circuits of Fig 2 to be quite useful. Input-capacitance

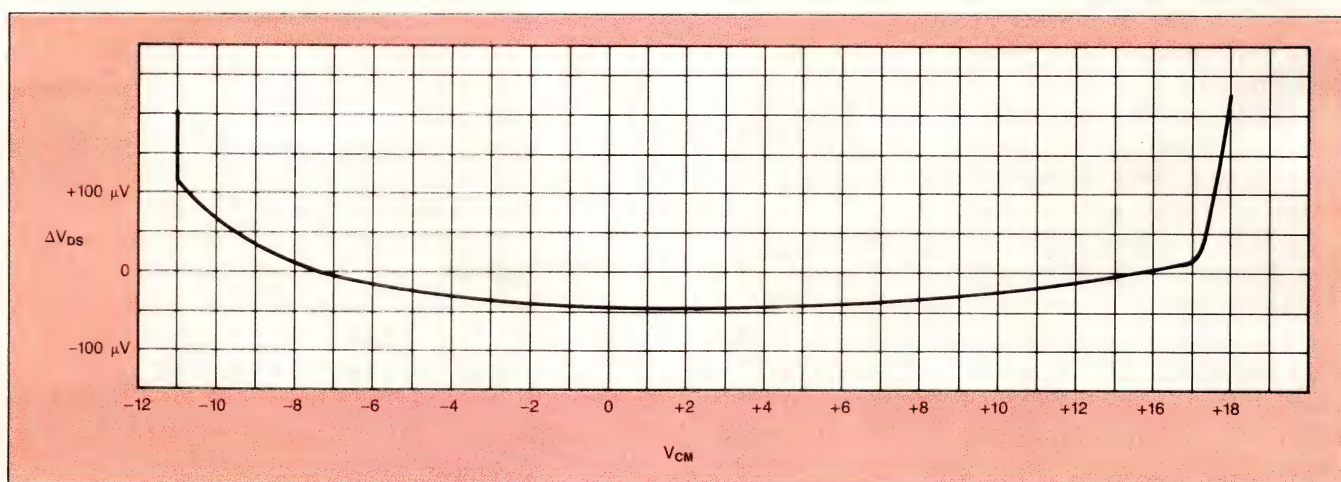


Fig 1—The CMRR of an op amp can't be represented by a single number. It makes more sense to look at the CMRR curve, ΔV_{OS} vs V_{CM} , and note its nonlinearities.

data is normally of interest only for high-impedance high-speed buffers or for filters where you want to make sure that the second-source device has the same capacitance as the op amps that are already working okay.

Recognize false "error" characteristics

Sometimes, an op amp may exhibit an "error" that looks like a bad problem, but isn't. For example, if an op-amp output is ramping at $0.3\text{V}/\mu\text{sec}$, you might be surprised when you discover that the inverting input, a summing point, is NOT at ground. Instead, it may be 15 or 30 or 100 mV away from ground. Why isn't the inverting input at the "virtual ground" that the books teach us? The virtual ground theory is applicable at dc and low frequencies, but if the output is moving

at a fast speed, then expecting the summing point to be exactly at ground is unreasonable. In this example, dV_{OUT}/dt equals $2\pi V_{\text{IN}}$ times the unity-gain frequency. So, 15 mV of V_{IN} is quite reasonable for a medium-bandwidth op amp, such as an LF356, and 50 or 70 mV is quite reasonable for a $\mu\text{A}741$. If you want an op amp to move its output at any significant speed, there has to be a significant error voltage across the inputs for at least a short time.

Also beware of op-amp models and what they might mistakenly tell you. For instance, the "standard" equation for a single-pole op amp's gain is $A = A_0/(1 + j\omega T_0)$. This equation implies that when the dc gain, A_0 , changes, the high-frequency gain, A , changes likewise. Wrong! With the growing popularity of computer modeling, I have to explain this to a would-be analyst every

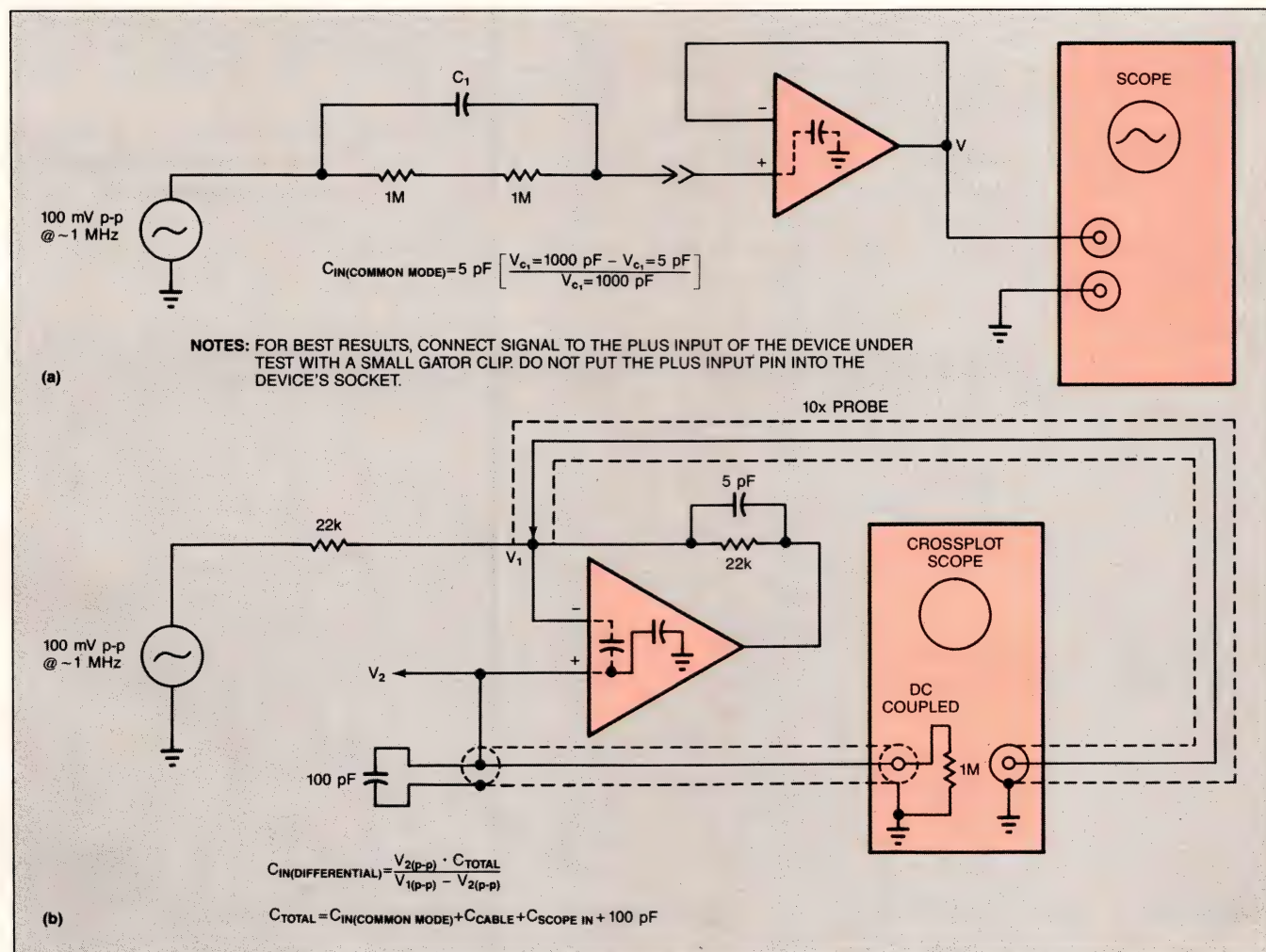


Fig 2—These circuits let you test an op amp's common-mode input capacitance (a) and differential input capacitance (b).

Don't expect the textbook "virtual-ground theory" to apply at high frequencies; for the output to slew rapidly, there must be an error voltage between the inputs.

month. NO, there is almost no correlation between the high-frequency response and the spread of dc gain. There are several ways to get an op amp's dc gain to change: Change the temperature, add on or lift off a load resistor, or swap in an amplifier with higher or lower dc gain. Although the dc gain can vary several octaves in any one of these cases, the gain-bandwidth product stays about the same. If there ever were any op amps whose responses *did* vary with the dc gain, they were abandoned many years ago as unacceptable.

So, your op-amp model is fine if it gives you a fixed gain-bandwidth product. But if the gain at 1 MHz doubles every time you double the dc voltage by reducing the load, you're headed for trouble and confusion. I once read an op-amp book that stated that when the dc gain changed, the first pole remained at the same frequency. In other words, the author claimed that the gain-bandwidth product increased with the dc gain. Wrong. I wrote to the author to object and to correct, but I never heard back from him.

I often see op-amp spec sheets in which the open-loop output impedance is listed as 50Ω . But by inspecting the gain specs at two different load-resistor values, you can see that the dc gain falls by a factor of 2 when a load of $1\text{ k}\Omega$ is applied. Well, if you have an op amp with an output impedance of $1\text{ k}\Omega$, its gain will fall

by a factor of 2 when you apply a $1\text{-k}\Omega$ load. But if its output impedance were 50Ω , as the spec sheet claimed, it would only fall 5%. So, whether it's a computer model or a real amplifier, be suspicious of output impedances that are unrealistically low.

Watch out for real trouble

What real trouble can an op amp get you into without much help from the components? Well, you could have a part with a bad V_{OS} . Or if the temperature is changing, the thermocouples of the op amp's Kovar leads may cause small voltages differences between the op-amp leads and the copper of the pc board. Such differences can amount to $1/10$ or $1/20$ of a Celsius degree times $35\text{ }\mu\text{V}$ per degree, which equals 2 to $3\text{ }\mu\text{V}$. A good way to avoid this problem is to put a little box over the amplifier to keep breezes and sunshine off the part. That's very helpful unless it's a high-power op amp. Then just repeat after me, "Heat is the enemy of precision," because it is.

You should remember, too, that not all op amps of any one type have the exact same output-voltage swing or current drive or frequency response. I get phone calls every four or five weeks from customers who complain, "We have a new batch of your op amps, and they don't have as good an output swing (or output

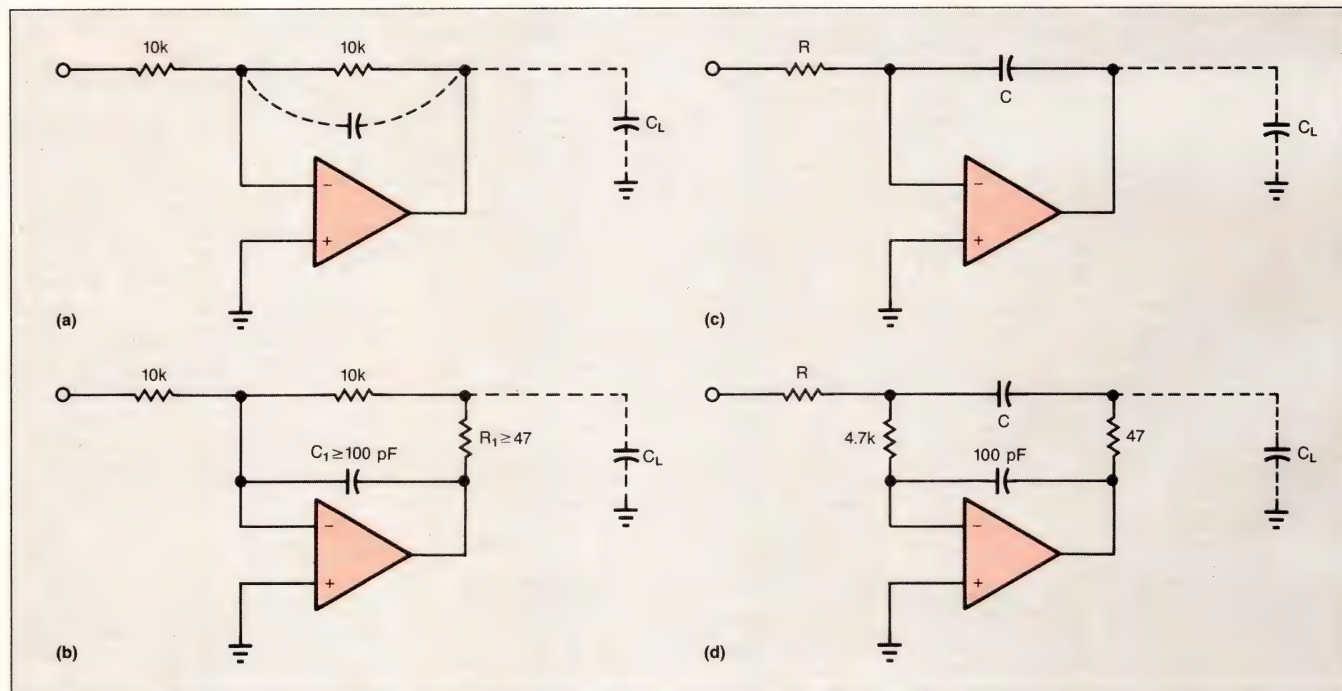


Fig 3—You can easily modify the basic inverter (a) and integrator (c) to decouple capacitive loads (b and d).

current or frequency response) as the previous batches." When I check it out, 98% of the time I find that a part with extremely good performance is just a random variation. The customer was in the habit of expecting the parts to be better than average. When they got some parts that were still much better than the guaranteed spec but worse than average or "typical," they found themselves in trouble. It's always painful to have to tell your friends that you love them when they trust you, but they really shouldn't trust your parts to always be better than average.

Oscillations often accompany op amps

One of the most troublesome problems you can have with op amps is oscillation. You can build an oscillator out of any gain block, but any gain block can also oscillate when you don't want it to. Op amps are no exception. Fortunately, most op amps these days are well behaved, and you only need to take four basic precautions to avoid oscillations.

First, always use power-supply bypass capacitors on each supply and install them near the op amp. For high-frequency op amps, the bypass capacitors should be very close to the device for best results. In high-frequency designs, you often need ceramic and tantalum bypass capacitors. Using bypass capacitors isn't just a rule of thumb, but a matter of good engineering and optimization.

Capacitive loads induce ringing

Second, avoid unnecessary capacitive loads; they can cause an op amp to develop additional phase shift, which causes the op amp to ring or oscillate. These effects are especially noticeable when you connect a 1x scope probe or add a coaxial cable or other shielded wire to an op amp to convey its output to another circuit. Such connections can add a lot of capacitance to the output. Unless you're able to prove that the op amp will be stable driving that load, you'd better add some stabilizing circuits. It doesn't take a lot of work to BANG the op amp with a square wave or a pulse and see if its output rings badly or not. You should check the op amp's response with both positive and negative output voltages because many op amps with pnp-follower outputs are less stable when V_{OUT} is negative or the output is sinking current.

I've seen pages of analysis that claim to predict capacitive-loading effects, but they're a complete waste of time. The output impedance of an op amp is usually not purely resistive. And if the impedance is low at

audio frequencies, it often starts to rise inductively at high frequencies, just when you need it low. Conversely, some op amps have a capacitive output characteristic, so when you add more capacitance on the output, the op amp just slows down a little and doesn't change its phase very much. But if an op amp is driving a remote, low-resistive load that has the same impedance as the cable, the terminated cable will be resistive at all frequencies and capacitive loading won't be a problem.

You can decouple an inverter's and integrator's capacitive load as shown in Fig 3. If you choose the components well, any op amp can drive any capacitive load from 100 pF to 100 μ F. The dc and low-frequency gain is perfectly controlled, but when the load capacitor gets big, the op amp will slow down and eventually have trouble slewing the heavy load. Good starting-point component values are $R_1=47\Omega$ and $C_F=100$ pF. These values usually work well for capacitive loads from 100 pF to 20,000 pF. If you have to make an integrator or a follower, you'll need an additional 4.7-k Ω resistor as indicated in Fig 3.

In some cases, as with an LM110 voltage follower,

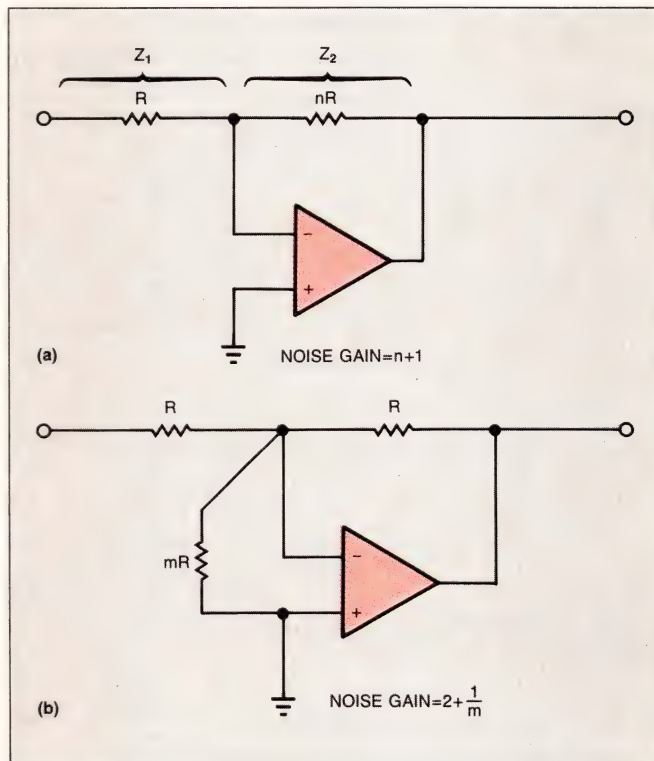


Fig 4—By adding just a single resistor, you can tailor the noise gain of a standard inverter.

Any gain block can oscillate, even when you don't want it to—op amps are no exception.

the feedback path from the output to the inverting input is internally connected and thus unavailable for tailoring. In this case, we can pull another trick out of our bag: the tailoring of noise gain. Noise gain is defined as $1/\beta$, where β is the attenuation of an op amp's feedback network. For instance, the β of the standard inverter configuration (Fig 4a) equals $Z_1/(Z_1 + Z_2)$, so the noise gain equals $N + 1$. You can raise the noise gain as shown in Fig 4b.

If you're using a low-noise-gain op-amp configuration, such as a unity-gain follower that has a noise gain of 1 (Fig 5a), it's obvious that for stability the op amp can't have appreciable phase shift out near its unity-gain frequency. If you can increase the noise gain to 4 or 5, the requirement for low phase shift eases considerably. No, you don't have to change the signal gain to 5. A noise gain of 5 or greater is easy to achieve (Fig 5b) while maintaining a gain of 1 for the signal. Even the unity-gain follower with a wire from the output to the inverting input can be saved, as illustrated in Figs 5c and d. You'll find a more complete description of these circuits in Ref 1. I should also mention that these concepts were used by Glenn DeMichele in his EDN Design Idea for which he won the 1988 Design Idea award (Ref 2).

My third recommendation to prevent oscillation in

general-purpose op amps is to add a feedback capacitor across R_F unless you can show that this capacitor isn't necessary. This capacitor's function is to prevent phase lag in the feedback path. Of course there are exceptions, such as the LF357 or LM349, which are stable at gains or noise gains greater than 10. Adding a feedback capacitor across the feedback paths of these op amps would be exactly the wrong thing to do.

Recently I observed that a number of National Semiconductor op-amp data sheets were advising feedback capacitor values of

$$C_F = \frac{C_{IN} R_{IN}}{R_F}$$

But, if you had an ordinary op amp whose C_{IN} was 5 pF and an inverter with a gain of -0.1 , this equation would tell you to use a C_F of 50 pF and accept a frequency response of 3 kHz. That would be absurd. If you actually build this circuit, you'll find that it works well with $C_F = 1.5$ pF, which gives the inverter a bandwidth of 100 kHz. So, we at NSC have just agreed to deep six that equation. We have a couple new formulas, which we've checked carefully, and we have found that you can get considerably improved bandwidth and excellent stability. For high values of

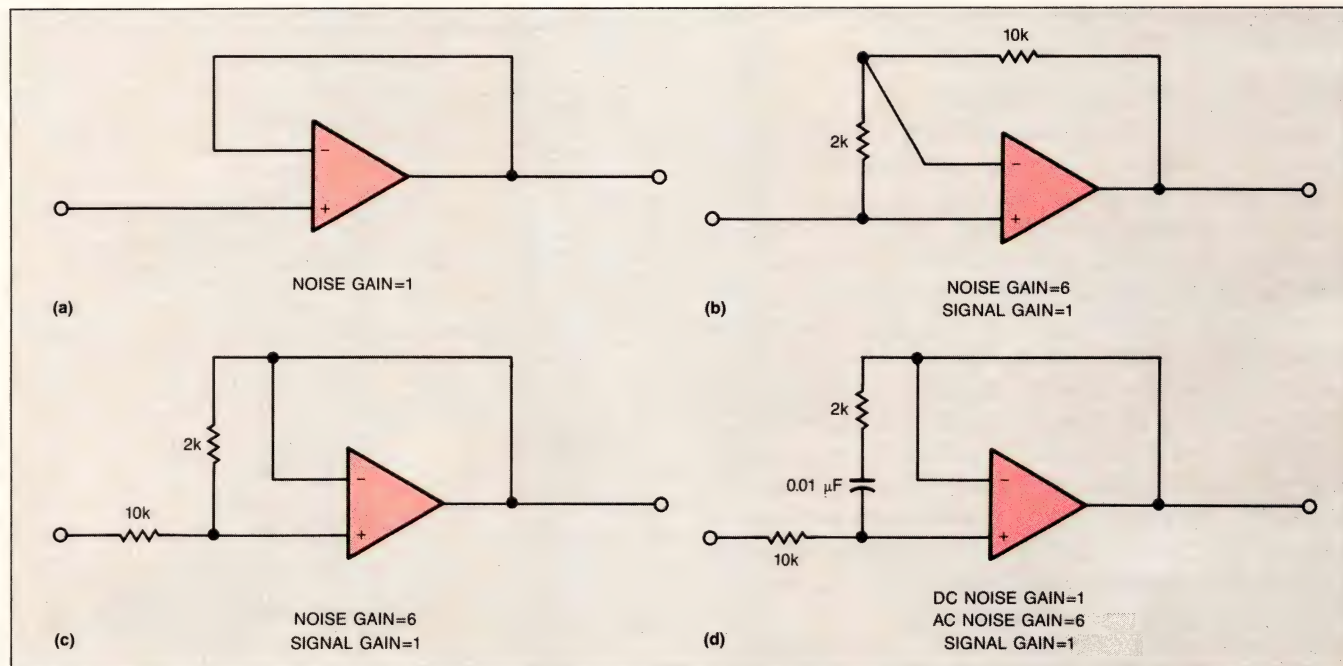


Fig 5—By manipulating the noise gain of an amplifier, you can stabilize unity-gain followers while maintaining the desired closed-loop gain.

gain and R_F , use the following equation:

$$C_F = \sqrt{\frac{C_{IN}}{GBW \times R_F}}$$

where GBW is the gain-bandwidth product. In those cases in which the gain or impedance is low, such as where

$$(1 + R_F/R_{IN}) \leq 2\sqrt{GBW \times R_F \times C_{IN}},$$

use the following equation:

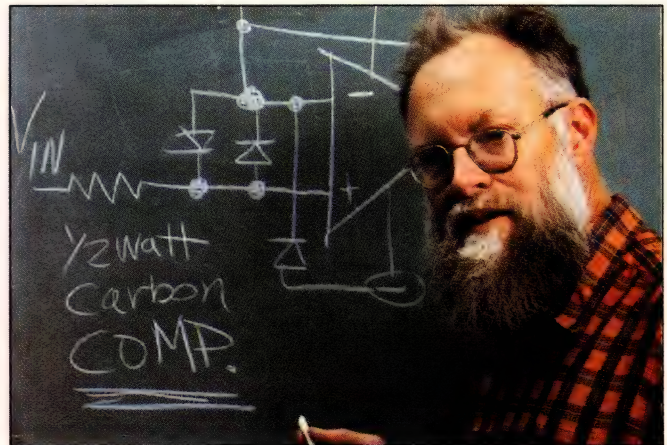
$$C_F = \frac{C_{IN}}{2 + 2 R_F/R_{IN}}$$

I won't bore you with the math, but these equations did come from real analytical approaches that have been around for 20 years—I championed them back at Philbrick Researches. The value of C_F that you compute is not that critical, it's just a starting point. You really must build and trim and test the circuit for overshoot, ringing, and freedom from oscillation. If the equation said 1 pF and you get a clean response only with 10 pF, you'd be suspicious of the formula. Note that when you go from a breadboard to a pc board, the stray capacitances can change, so you must recheck the value of C_F . In some cases, you may not need a separate capacitor if you build 0.5 pF into the board.

My last recommendation is that when you think the circuit is okay—that is, free from oscillation—test it anyway per Pease's Principle (see **box**) to make sure it's as fast or stable as you expect. Be sure that your circuit isn't ringing or oscillating at any expected operating condition or load or bias.

In addition to oscillatory behavior, another problem you might have when using op amps is noise. Most op amps have fairly predictable noise. It's often right down at theoretical levels, especially at audio frequencies. There's a pretty good treatment of noise and its effects in various applications in Thomas Frederiksen's book (**Ref 3**). Also, if you want to optimize the noise for any given source resistance or impedance, National Semiconductor's Linear Applications Note AN222 (**Ref 4**) has some good advice as does the article in **Ref 5**.

You'll have difficulty with noise when it's unpredictable or when op amps of a particular type have varying noise characteristics. This problem rarely happens at audio frequencies but is likely to happen sporadically at low frequencies, such as 10 or 100 Hz or even lower



Photographs by Peggi Willis

External components determine an op amp's operation, and you can often keep a circuit out of trouble only by using components with characteristics that aren't found in books or data sheets.

frequencies. Every manufacturer of transistors and amplifiers tries to keep the noise low, but occasionally some noisy parts are built. Sometimes the manufacturer is able to add tests that screen out the noisy parts. But these tests aren't cheap if they take even one second of tester time, which may cost three cents or more.

Beware of popcorn noise

Flicker noise, also known as 1/f noise, is ac noise that exists at low frequencies. And even more insidious than 1/f noise is popcorn noise—a type of electrical noise in which bursts of square steps are added to the normal thermal noise at random times. Popcorn noise occurs rarely these days; but, unfortunately, it's not at 0%, not even with the cleanest processing and the best manufacturers. I've been chastised and told that some of my amplifiers are noisy compared with those of certain competitors. But when I look at the competitor's data and plots, I see 1/f and popcorn noise lurking unnoticed in a corner. On high-performance parts, we try to screen out the noisy ones. But when a few parts have a spacing of two to 10 seconds between bursts of popcorn, it's not cost effective to look for those parts. Only a small percentage of our customers would want to reject that part AND pay for the testing. Remember, 10 seconds of testing time equals 30 cents; time equals money.

Although oscillation and noise problems may be the most common ones you'll encounter when you use op amps, there's a host of other characteristics that are helpful to look out for. These characteristics include

To avoid oscillations, use bypass and feedback capacitors, avoid or compensate for heavy capacitive loads, and apply Pease's Principle.

overload or short-circuit recovery, settling time, and thermal response. Many op amps have a fairly prompt recovery from overdrive when you make the output go into the stops—that is, when you force the output too close to the power-supply rails. For most op amps, this recovery characteristic is not defined or specified. One recently advertised op amp requires only 12 nsec to come out of the stops. Just about all other op amps are slower to one degree or another. The recovery time for chopper-stabilized amplifiers can be seconds.

Even if you have a fast op amp that doesn't have a delay coming out of limit, there may be circuits, such as integrators, that take a long time to recover if you overdrive the output and inputs. To avoid these cases, a feedback bound made of zeners and other diodes may be helpful (Ref 6). However, if you have a differential amplifier, you may not be able to use any zener diode feedback limiters. I recall the time I designed a detector circuit using a fast, dielectrically isolated op amp. When I went to put it into production, nothing worked right. It turned out that the manufacturer had just recently redesigned the chip to cut the die size by

50%. The new and improved layout slowed down the op amp's overdrive-recovery time. I wound up redesigning the circuit to use an LM709. I saved a lot of pennies in the long run, but the need to change parts didn't make me very happy at the time.

Rely only on guaranteed specs

Don't rely on characteristics that aren't specified or guaranteed by the manufacturer. It's perfectly possible for you to test a set of samples and find that they feature some desired performance characteristic that is not specified by the manufacturer. But if the next batch doesn't fulfill your requirements, whom are you going to get angry at? Don't get mad at me, because I'm warning you now. Any unspecified conditions may cause a test result to vary considerably compared to a guaranteed tested specification. If you have to work in an unspecified range, you should keep a store of tested good ICs in a safe as insurance. If a new batch comes in and tests "bad" you'll have some backup devices.

I recall a complaint from a user of LM3046 transistor

Pease's Principle

For many years, I've been cautioning people: If you have a regulator or an amplifier circuit and it oscillates, DO NOT just add resistors or capacitors until the oscillation stops. If you do, the oscillation may go away for a while, but after it lulls you into complacency, it will come back like the proverbial alligator and chomp on your ankle and cause you a great deal of misery.

Instead, when you think you have designed and installed a good fix for the oscillation, BANG on the output with square waves of various amplitudes, frequencies, and amounts of load current. One of the easiest ways to perform this test is to connect a square-wave generator to your circuit through a couple hundred ohms in series with a 0.2- μ F ce-

ramic disc capacitor. Connect the generator to the scope, so you can trigger on the square-wave signal. Also, apply an adjustable dc load that's capable of exercising the device's output over its full-rated output-current range or, in the case of an op amp, over its entire rated range for output voltage AND current.

To test an op amp, try various capacitive loads to make sure it can drive the worst case you expect it to encounter. For some emitter-follower output stages, the worst case may be around 10 to 50 pF. The oscillation may disappear with heavier capacitive loads.

When you BANG a device's output and that output rings with a high Q, you know your "fix" doesn't have much margin. When

the output just goes "flump" and doesn't even ring or overshoot appreciably, you know your damping is effective and has a large safety margin. Good! Now, take a hair dryer and get the circuit good and warm. Make sure that the damping is still pretty well behaved and that the output doesn't begin to sing when you heat the capacitor or power transistor or control IC or ANYTHING.

I don't mean to imply that you shouldn't do a full analysis of ac-loop stability. But the approach I have outlined here can give you pretty good confidence in about five minutes that your circuit will (or won't) pass a full set of exhaustive tests.

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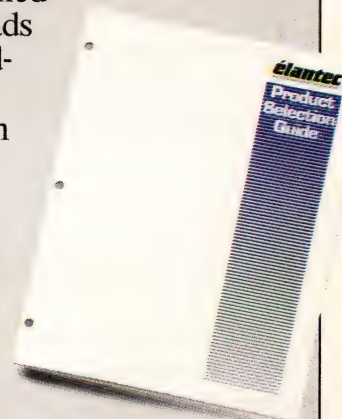
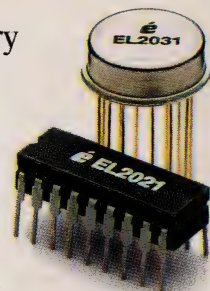
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To get the most out of the time you spend troubleshooting, thoroughly understand a problem before squashing it and moving on to the next.

arrays: A fraction of the parts failed to log accurately over a wide range. The "bad" ones turned out to have a beta of 20 at a collector current of 50 pA, versus a beta of 100 for the "good" ones. I convinced the user that keeping a few hundred of these inexpensive parts in a safe (yes, literally) would be a lot cheaper than getting the manufacturer to sort out high- β devices.

Op amps and other linear ICs can also have errors due to thermal tails. These tails occur when the change of heat in one output transistor causes a thermal gradient to sweep across the chip. This change occurs gradually, often over milliseconds, and causes uneven heating of input transistors or other sensitive circuits. Many high-power circuits and precision circuits, such as the LM137, are tested these days for thermally caused error. These tests aren't performed just on power ICs, but also on precision references and instrument-grade op amps. In fact, a recent article by a Tektronix engineer (Ref 8) points out that thermal tails can be a major source of error in fast signal amplifiers and that innovative circuit design can minimize those overdrive-recovery errors.

These days, just about every manufacturer's monolithic op amps will survive a short from the output to ground. (Hybrids are often unprotected.) But it's not always clear whether an op amp will survive a short circuit to the positive or negative supply or, if so, for how long. You may have to ask the manufacturer, and you can expect some kind of negative answer. You'll be told to avoid overheating the device above its absolute maximum junction temperature. Even if an amplifier or regulator does recover fairly quickly from current limit, nobody will guarantee that it won't oscillate when in current limit. Nor will the manufacturer have much knowledge about how the circuit recovers from the thermal gradients caused by current limit. If an op amp survives a high-power overload, it's not fair to ask the device to recover its full accuracy very quickly. The most you really can ask for is that it survives with no degradation of reliability—that's the standard.

Some op amps, but mostly voltage regulators and other linear ICs, have an on-chip temperature limiter. Thermal shutdown circuits can improve reliability. If a heavy overload is applied for a long time, or there is no heat sink, or the ambient is just too hot, these circuits detect when the chip's temperature exceeds 150°C and then turn off the output. The thermal-limiter circuit in the LM117 and other early power ICs just decreased the output current to a safe dc value to hold



When you're trying to troubleshoot a one-of-a-kind circuit, it helps if you can remember how the circuit is supposed to operate. A little bit of documentation and a schematic with some scribbled notes can save you a lot of grief.

the die temperature to around 160°C. In other cases, these thermal limiters oscillate On and Off with a duty cycle that ensures the 160°C chip temperature. As we at NSC were about to design the LM137, we looked back and decided the latter characteristic was preferable, so we designed about five degrees of thermal hysteresis into the thermal-limit circuit. That way, the circuit makes a strong attempt to restart its heavy load with a repetition rate of about 100 Hz.

So, we actually designed an oscillation into this thermal-limit circuit, but we never bothered to mention it on the data sheet. H'mmm, we shouldn't be so sloppy. I apologize. I'll do better next time. (This situation has a bearing on one of my pet peeves: bad data sheets. I get really cross about bad ones, and I really do try hard and work hard to make good ones. Refer to "How to Read a Data Sheet" (Ref 9) because bad data sheets can get the user into trouble.)

Different methods uncover different errors

Now that you know some op-amp problems to look out for, how do you actually troubleshoot an op-amp circuit? I usually split my plan along two lines: ac and dc problems. Examples of ac problems include oscillations and ringing; dc problems include bad errors and pegged outputs, which are outputs stuck at either the positive or negative supply rail. Obviously, you need a scope to be sure the circuit isn't oscillating. It always makes me nervous when I find out that the customer I'm trying to help DOESN'T EVEN HAVE A SCOPE. I can understand if an engineer only has a crummy

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scope, but there are certain problems you cannot expect to solve—nor can you even verify a design—if you don't have a scope.

If the problem is an ac problem, I first make sure that the input signals are well behaved and at the values I expect them to be. Then I put my scope probes on all the pins and nodes of the circuit. Sometimes it's appropriate to use a 10x probe, and other times I shift to 1x mode. Sometimes I ac couple the scope; sometimes I dc couple it. I check all the pins, especially the power-supply pins. Then—depending on what clues I see—I poke around and gather symptoms by adding capacitors or RC boxes to assorted circuit nodes. I try to use two probes to see if the input and output have an interesting phase relationship, and I simultaneously verify that the output is still oscillating.

Many of the techniques I use depend on whether the circuit is one I've never tried before or one that I see all the time. Sometimes I find an unbelievable situation, and I make sure that I understand what's going on before I just squash the problem and proceed to the next. After all, if I'm fooling myself, I really ought to find out how or why so I won't do it again.

If the op amp exhibits a dc error or a peg, I first check with my scope to see that there's no oscillation. Then I bring in my 5-digit DVM and scribble down a voltage map on a copy of the schematic. On the first pass, I'm likely to just keep the numbers in my head to see if I can do a quick diagnosis of a problem that's obvious. Failing that, I start writing meticulous notes to help look for a more insidious problem. I look at the numbers on the schematic and try to guess the problem. What failure could cause that set of errors? A resistor of the wrong value? A short? An open? Then I try to cook up a test to confirm my theory. Sometimes I have to disconnect things, but I try to minimize that. Sometimes adding a resistor or voltage or current will yield the same result, and it's much easier than disconnecting components.

If an amplifier circuit isn't running at all, sometimes the right thing to do is to reach into the circuit and "grab" one amplifier's input and force it to go above and below the other input. If the output doesn't respond at all, you have a dead amplifier, an amplifier with no connections, or a stuck output. This open-loop test is not obvious, but its results are.

Many of these op-amp troubleshooting tips are applicable to other components as well. The next article in this troubleshooting series will continue with buffers, comparators, and related devices.

EDN

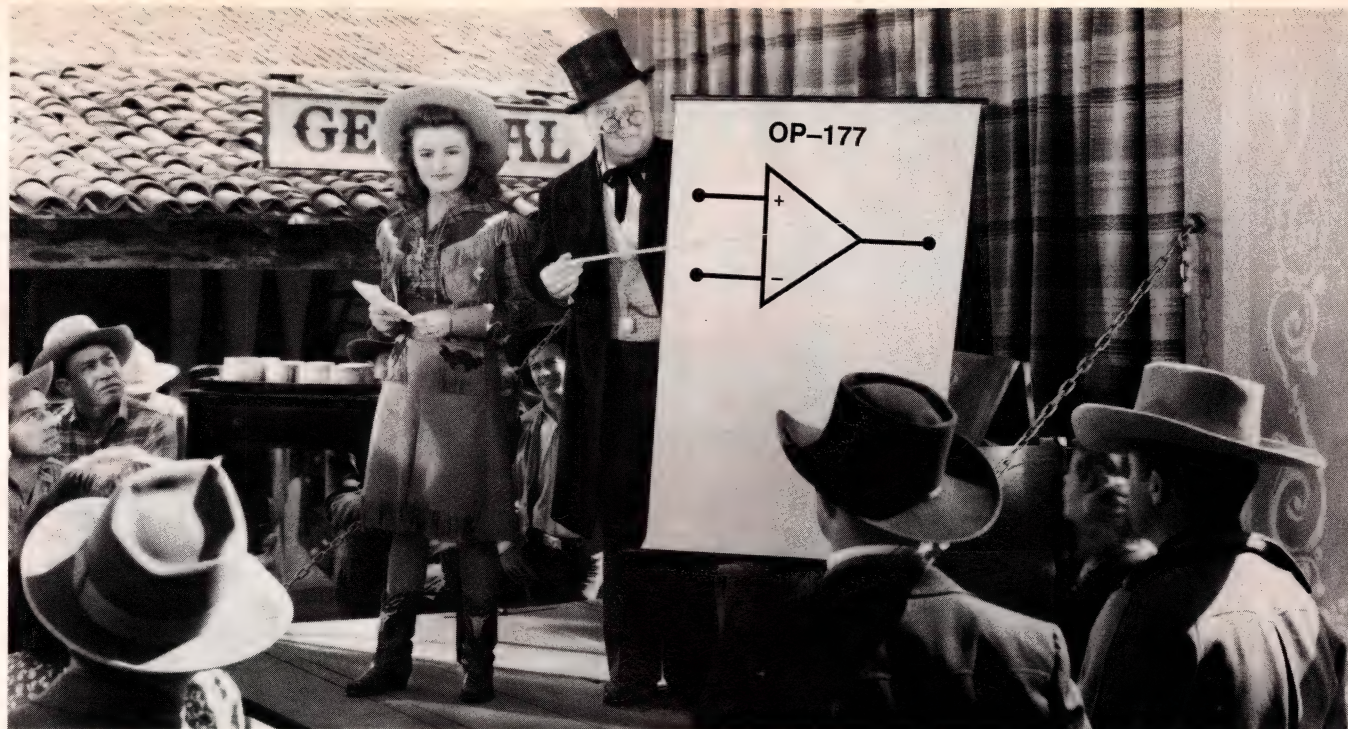
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Author's biography

For information about Bob Pease, see the **box**, "Who is Bob Pease, anyway?" on page 148 of the January 5, 1989, edition of *EDN*.

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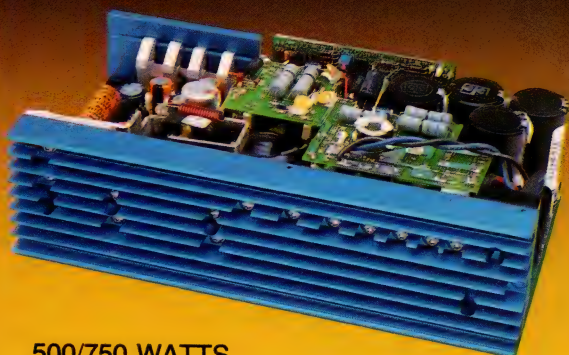
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September 1989

Guy Hoover
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Circuit Description

The LTC1090 is a 10-bit data acquisition system with an eight channel multiplexer. The channel to be read is software selectable and all channels can be referred to the COM pin. In the circuit of Figure 1, CH0 is used to servo the COM pin giving the user a seven channel, offset corrected data acquisition system.

Figure 2 shows how the processor serves the COM pin to eliminate the A/D offset. CH0 is set to a 0.5 LSB voltage. The COM pin is servoed (by the pulse width modulated signal on

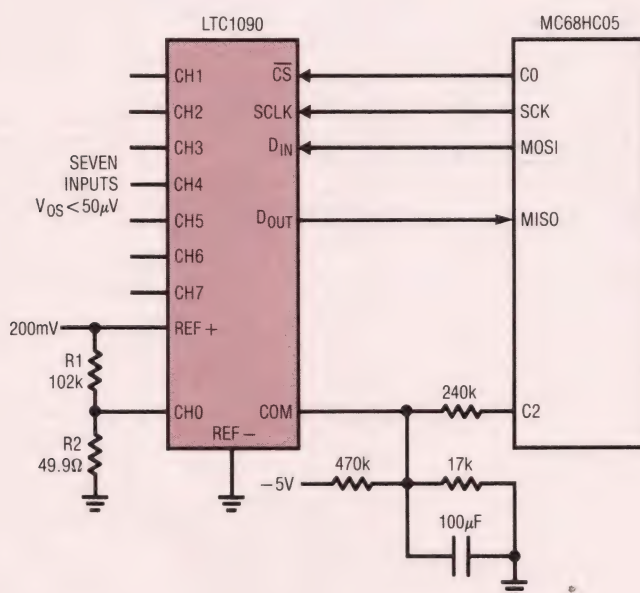


Figure 1. Circuit Provides Seven Channel 10-Bit Data Acquisition System with Less than 50 μ V of Offset

port C2) so that the CH0 reading dithers between 0 and 1 LSB. The $100\mu\text{F}$ filters the PWM signal at the COM pin. Motorola MC68HC05 code is available from LTC to correct the LTC1090 offset and read the remaining seven channels. This algorithm

will work in either unipolar or bipolar mode. (Unipolar is shown. For bipolar the 49.9Ω resistor is changed to 100Ω and the decision block is changed to " $\text{CH0} \leq 0$?")

After initializing the processor, the code sends a D_{IN} word to the LTC1090 requesting CH0 to be read with respect to COM. The next D_{IN} word that is sent will set up the A/D for the desired channel to be read while the CH0 data previously requested is shifted into the processor. If the CH0 D_{OUT} is 0 then C2 is cleared. If the CH0 D_{OUT} is greater than 0 then C2 is set. Another D_{IN} word requesting CH0 data is sent and the D_{OUT} data from the previously requested channel is read into the processor.

As can be seen from the LTC1090 data sheet the linearity and full scale errors with a 200mV full scale voltage are still within 0.5 LSB. To fully take advantage of the reduced offset of the auto-zero circuit the noise of the LTC1090 must be reduced. This can be done by averaging the data with the processor. Figure 3 shows a dynamic cross plot of the output data near half-scale after 64 averages. The top trace is the B9 transition of the LTC1090 while the bottom trace is a binary weighted summation of B0 and B1. The horizontal scale is 1 LSB per major division. The averaged noise is much less than 1 LSB.

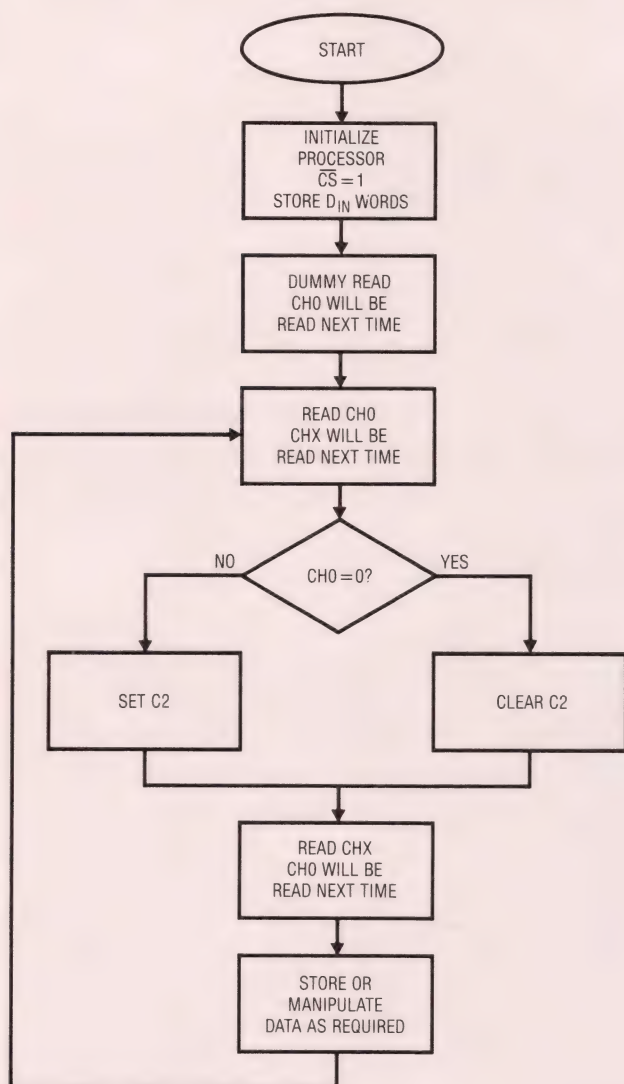


Figure 2. Auto-Zero Flowchart

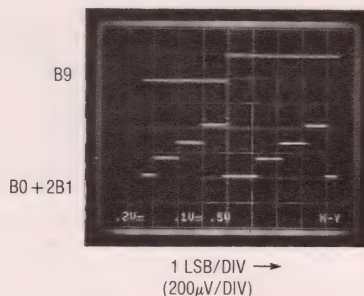
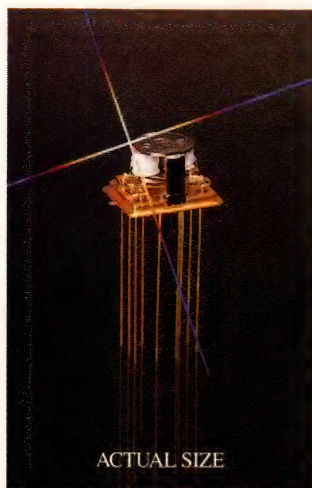


Figure 3. Dynamic Cross Plot Shows Excellent LTC1090 Performance with Only 200mV Full Scale

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DESIGN IDEAS

EDITED BY CHARLES H SMALL

Intermittent converter saves power

Paul D Gracie

The Microdoctors Inc, Palo Alto, CA

The circuit in **Fig 1** switches its dc/dc converter, IC₁, off whenever the large filter capacitor, C₆, has sufficient charge to power the load. This scheme, which proves especially useful for battery-powered systems, saves power because virtually all dc/dc converters have poor efficiency at low and zero output-power levels.

This particular circuit uses a dc/dc converter that produces 115V dc from a 9V-dc input; you can tailor the circuit to suit other converters. The heart of the circuit is a 555 timer configured as a dual-limit comparator. An input of less than $\frac{1}{3} V_{CC}$ to pin 2 of the 555 turns the output, pin 3, on; an input of more than $\frac{2}{3} V_{CC}$ to pin 6 turns the output off. Thus, the 555 turns the converter on or off, depending on the voltage across C₆. The 555's complementary output lights the charge LED when the FET is on.

Initially, the voltage on C₆ is zero, and the 555's output turns on the FET, Q₁. Q₁, in turn, enables the converter to run, which charges up C₆. When the voltage on the capacitor reaches the value set by R₃, the 555 turns off the converter. Then C₆ slowly discharges into the combined load of the voltage divider (R₂, R₃,

and R₄) and the reverse-biased blocking diode, D₁.

When the voltage falls below $\frac{1}{3} V_{CC}$, the 555 restarts the dc/dc converter. If this circuit powers a load that periodically goes into a zero-power, shut-down mode, the 555 switches the dc/dc converter on full time whenever the load kicks in.

The 78L05 voltage regulator stabilizes the 555's internal resistive divider in the face of varying battery voltages. The regulator also enables the circuit to detect low battery voltage. When the supply voltage falls below 7.5V, the output of the converter is no longer high enough to charge the capacitor to the upper set point; hence, the charge LED no longer lights.

The circuit uses 205 mA when the converter is on and 10 mA when the converter is off. The duty cycle comprises a 5-sec on period and a 150-sec off period and represents a 92% power reduction. You can further reduce power consumption by removing the charge LED and using a CMOS 555 and a CMOS 78L05 regulator.

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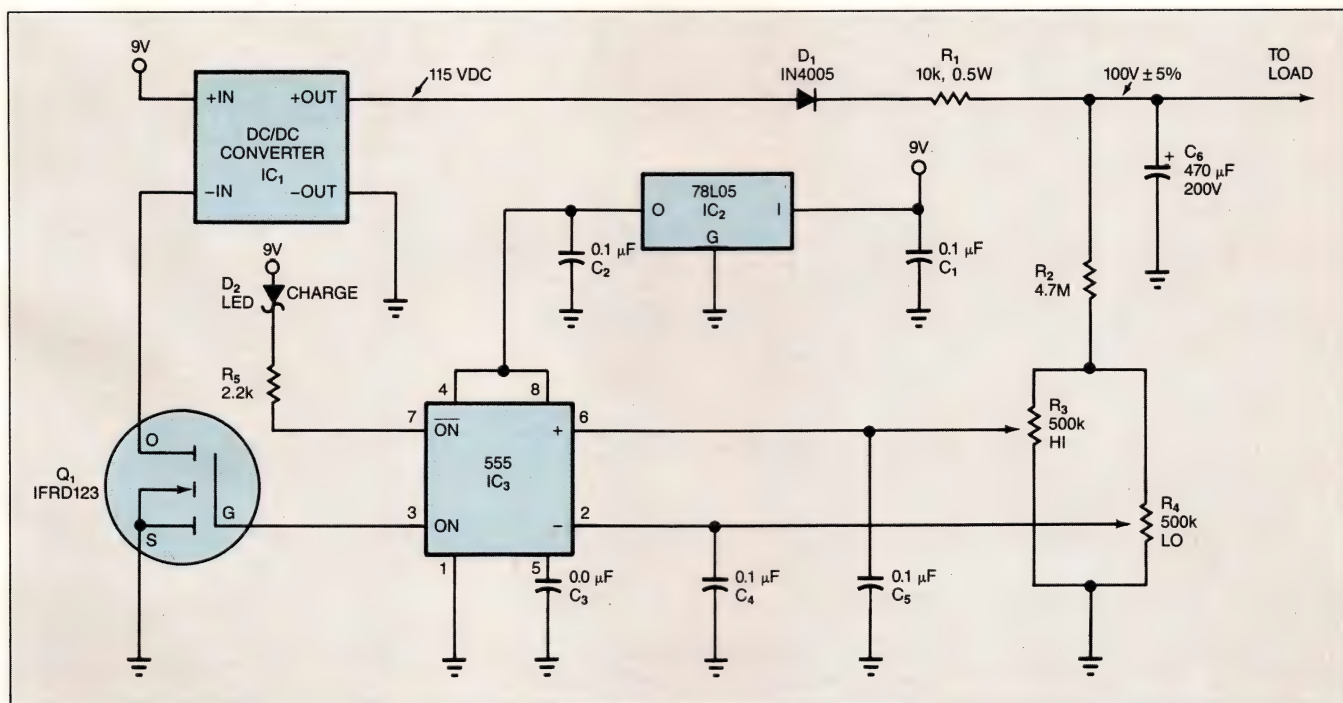


Fig 1—Employing a 555 timer acting as a dual-limit comparator, this circuit reduces low- and no-load power consumption by switching off the dc/dc converter when the filter capacitor is charged up.

Temperature controller has defrost cycle

Xiang-yang Zhou and Tung Jing
Hefei Polytechnic University,
Hefei, People's Republic of China

The temperature controller in Fig 1 works over a temperature range of -50 to $+150^{\circ}\text{C}$ and permits defrosting. Potentiometers R_7 , VR_3 , and R_8 set the controller's normal-cycle trip point, and R_5 and R_6 set the normal-cycle hysteresis range (Fig 2). Switch S_1 initiates defrosting, switch S_2 cancels defrosting, and potentiometers VR_1 and VR_2 set the defrost-temperature trip point.

The LM134, IC_1 , is a thermal sensor. One section of IC_3 , a quad op amp, buffers the sensor's output. The other sections function as a Schmitt trigger and buffer for the normal-cycle circuitry and as a comparator for the defrost-cycle circuitry. If you wish to control a heater rather than a refrigerator, omit the final inverter in Q_1 's base circuit. You must select LM7805s

that have outputs between 4.95 and 5.05V, or the circuit may not work. **EDN**

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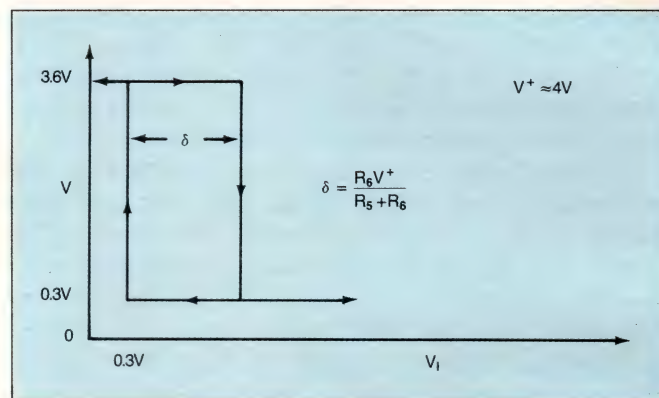


Fig 2—Resistors R_5 and R_6 determine the temperature controller's normal-cycle hysteresis range.

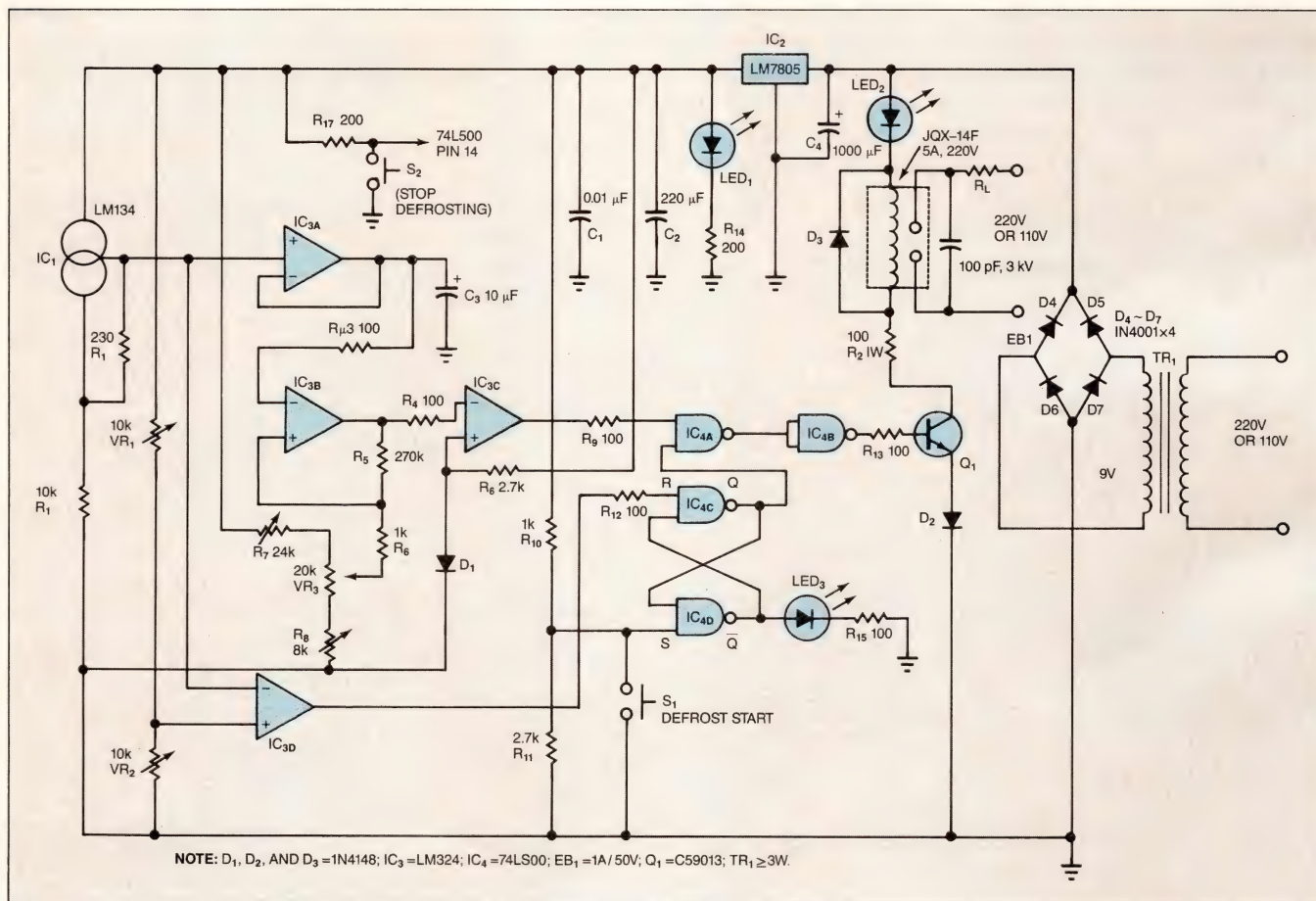


Fig 1—This temperature controller provides a defrost cycle.

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Switch fast... to Mini-Circuits' GaAs switches.

SPECIFICATIONS

Pin Model,	KSW-2-46		KSWA-2-46	
Connector Version	ZFSW-2-46		ZFSWA-2-46	
FREQ. RANGE	dc-4.6 GHz		dc-4.6 GHz	
INSERT. LOSS (dB)	typ	max	typ	max
dc-200MHz	0.9	1.1	0.8	1.1
200-1000MHz	1.0	1.3	0.9	1.3
1-4.6GHz	1.3	1.7	1.5	2.6
ISOLATION (dB)	typ	min	typ	min
dc-200MHz	60	50	60	50
200-1000MHz	45	40	50	40
1-4.6GHz	30	23	30	25
VSWR (typ)	ON	1.3:1	1.3	
	OFF	—	1.4	
SW. SPEED (nsec)				
rise or fall time	2(typ)		3(typ)	
MAX RF INPUT (bBm)				
up to 500MHz	+17		+17	
above 500MHz	+27		+27	
CONTROL VOLT.	-8V on, OV off		-8V on, OV off	
OPER/STOR TEMP.	-55° to +125°C		-55° to +125°C	
PRICE (10-24)	\$32.95		\$48.95	
	\$69.95		\$79.95	

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CIRCLE NO 90

Test finds zero-TC current of zener diodes

Irwin Cohen

Hewlett-Packard, Rockaway, NJ

The data sheets of reference zener diodes such as the 1N825 specify a value of current at which the zener has a zero temperature coefficient. This stated current is an average value and is not generally the actual zero-TC current of the zener. By using the simple setup shown in **Fig 1**, you can determine the actual zero-TC current of a specific zener diode in less than 60 seconds. In order to determine the zero-TC current for a particular zener diode, you must gather V-I data at two temperatures; the point at which the two curves intersect is the zero-TC point.

To find the V-I characteristic at room temperature, the HP Basic program in **Listing 1** causes the HP6625A programmable power supply to increase the diode's current in 250- μ A steps to as high as 15 mA. Using the precision readback capability of the HP6625A, the program measures and stores the resulting voltages.

During the next 45 seconds, the program causes the supply to run 400 mW of power into the zener, which heats its junction to approximately 150°C. The exact temperature is not important; it simply must be some

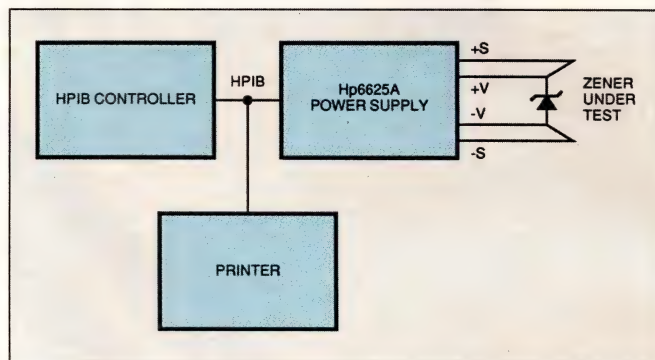


Fig 1—This test setup enables you to find the value of current at which a zener diode exhibits zero temperature coefficient; a Basic program causes the supply to step the current and then measure the voltage drop across the zener. By comparing the V-I data generated at both room temperature and high temperature, the program finds the zero- or minimum-TC current.

high junction temperature that doesn't exceed the diode's maximum junction temperature. At the end of this heating period, the program causes the HP6625A to repeat the previously described sequence of current tests. These data points represent the V-I characteristic of the heated junction.

At this point, the program prints out both sets of

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DESIGN IDEAS

V-vs-I data as well as the differences between the voltages recorded at each current level. The true zero TC is found at the point where the voltage difference is zero. In addition, both the V-I curves and the difference between them are plotted as a function of the zener current. If the zener under test has no point of zero TC, the data indicates the point of minimum TC.

If you need greater accuracy, you can alter the program to increment the current in steps as small as 1

μ A, which is the resolution of the HP6625A. Note that this modification will lengthen the amount of time necessary to complete the test. You can also use an external, HP-IB-compatible DVM to measure the zener voltage, thus achieving a resolution greater than 500 μ A.

EDN

To Vote For This Design, Circle No 525

LISTING 1—TC TEST PROGRAM

```
10 ! THIS PROGRAM WILL PRINT THE POINTS OF THE V-I CHARACTERISTICS
20 ! OF A ZENER DIODE (<7V) AT JUNCTION TEMPS. OF APPROX. 25 & 150 DEG-C.
30 ! ITS ASSUMED THAT THE TEST IS RUN AT 25 DEG-C.
40 ! THE DIFF. BETWEEN THESE TWO CURVES WILL ALSO BE PRINTED.
50 ! ZERO T.C. OCCURS WHEN THE DIFF. BETWEEN CURVES IS ZERO.
60 ! HP-IB ADDRESS OF HP6625A SUPPLY=705.
70 !
80   DIM A(60)
90   DIM B(60)
100  OUTPUT 705;"ISET 1,0" ! CURRENT SET TO ZERO INITIALLY
110  OUTPUT 705;"IRSET 1,.015" !CURRENT RANGE SET TO .015A
120  OUTPUT 705;"VRSET 1,7" !VOLTAGE RANGE SET TO 7 VOLTS
130  OUTPUT 705;"VSET 1,7" ! VOLTAGE SET TO 7 VOLTS-CONSTANT CURRENT MODE
140  !
150  ! 60 TEST POINTS TAKEN IN INCREMENTS OF .25ma.
160  FOR X=1 TO 60
170    OUTPUT 705;"ISET 1";X/4000
180    OUTPUT 705;"VOUT? 1"
190    ENTER 705;Vz
200    A(X)=Vz
210  NEXT X
220  !
230  ! ZENER RUN AT 400mw DISIPATION FOR 45 SEC.
240  OUTPUT 705;"IRSET 1,.5" ! CURRENT RANGE SET TO .5A FOR POWER MODE
250  T=TIMEDATE
260  WHILE TIMEDATE-T<45
270    Iz=.4/Vz
280    OUTPUT 705;"ISET 1";Iz
290    OUTPUT 705;"VOUT? 1"
300    ENTER 705;Vz
310  END WHILE
320  !
330  !AT END OF HEATING INTERVAL TEST POINTS REPEATED & STORED
340  OUTPUT 705;"IRSET 1,.015" ! CURRENT RANGE SET TO .015A
350  FOR X=1 TO 60
360    OUTPUT 705;"ISET 1";X/4000
370    OUTPUT 705;"VOUT? 1"
380    ENTER 705;Vzz
390    B(X)=Vzz
400  NEXT X
410  OUTPUT 705;"ISET 1,0" !CURRENT SET TO ZERO
420  !
430  !PRINT RESULTS
```


DESIGN IDEAS

LISTING 1—TC TEST PROGRAM *(continued)*

```
440  PRINTER IS 701
450  ! Iz is in amps, Vz=cold Zener voltage,Vzh=heated Zener voltage
460  ! DELTA=Vzc-Vzh
470  PRINT "Iz","Vzc","Vzh","Vzc-Vzh","MAX. Pd=.4W"
480  FOR X=1 TO 60
490      PRINT X/4000,A(X),B(X),A(X)-B(X)
500  NEXT X
510  ! PLOT OF DELTA vs. CURRENT
520  GINIT
530  GCLEAR
540  DEG
550  GRAPHICS ON
560  LDIR 0
570  WINDOW -1.5,10,-.001,.001 ! -1.5-10ma. (X axis),-1mv to +1mv. (Yaxis)
580  AXES .5,.0001 ! .5ma./div (X axis), .1mv./div (Y axis)
590  MOVE 6,-.0002
600  LABEL ".5ma./div"
610  MOVE 6,.0005
620  LABEL "Vzc-Vzh vs. Iz"
630  MOVE -.5,.00015
640  DEG
650  LDIR 90
660  LABEL ".1mv./div"
670  FOR X=1 TO 60
680      Y=A(X)-B(X)
690      PLOT X/4,Y
700  NEXT X
710  DUMP GRAPHICS
720  PENUP
730  GCLEAR
740  LDIR 0
750  WINDOW -1.5,10,5.8,6.5 ! Y axis window 5.8v TO 6.5v
760  AXES .5,.1,0,5.9 ! expanded Y axis starts at 5.9v
770  FOR X=1 TO 60
780      PLOT X/4,A(X)
790  NEXT X
800  PENUP
810  FOR X=1 TO 60
820      PLOT X/4,B(X)
830  NEXT X
840  MOVE 5,5.85
850  LABEL ".5ma./div"
860  LDIR 90
870  MOVE -.5,6.2
880  LABEL ".1v/div"
890  LDIR 0
900  MOVE -1.5,5.9
910  LABEL "5.9v"
920  MOVE 7,6.2
930  LABEL "Vzc & Vzh vs. Iz"
940  DUMP GRAPHICS
950  PRINTER IS CRT
960  END
```


Design Entry Blank

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The winning Design Idea for the May 11, 1989, issue is entitled "Amplitude-locked loop speeds filter test," submitted by Steven C Hageman of Calnex Manufacturing Co Inc (Pleasant Hill, CA).

Your vote determines this issue's winner. All designs published win \$100 cash. All issue winners receive an additional \$100 and become eligible for the annual \$1500 Grand Prize. **Vote now**, by circling the appropriate number on the reader inquiry card.

DESIGN IDEAS

FEEDBACK AND AMPLIFICATION

Idea risks copyright violation

A recent Design Idea, "Single-chip μ P acquires Basic" (EDN, April 27, 1989, pg 221) by G Nagendra Rao, shows how to extract the object code from an Intel 8052AH-BASIC single-chip μ P, so that the code can be loaded into a CMOS PROM and run on a CMOS 80C52.

This idea is valid and interesting, but there are two points that should be mentioned.

First, the code is probably copyrighted. I don't claim to be a legal expert, but I doubt that Intel would approve of such duplication without a licensing agreement.

Second, the 80C52-BASIC, a CMOS equivalent of the Intel device, is available from Micromint Inc, Vernon, CT, for \$14.50 (100).

*Carl Spearow, Senior Engineer
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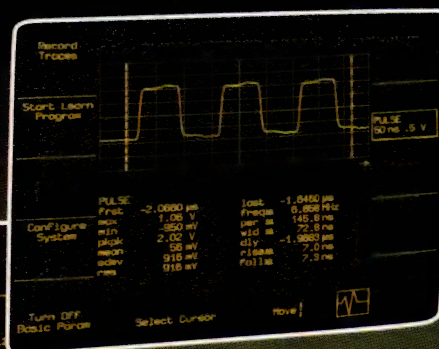
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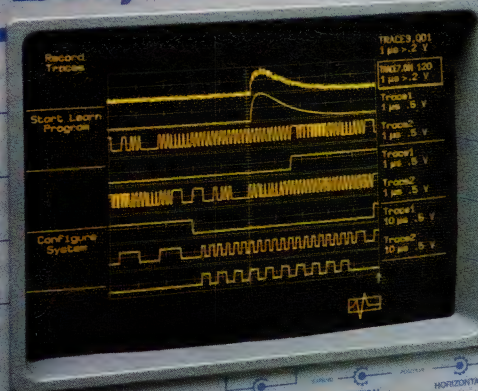
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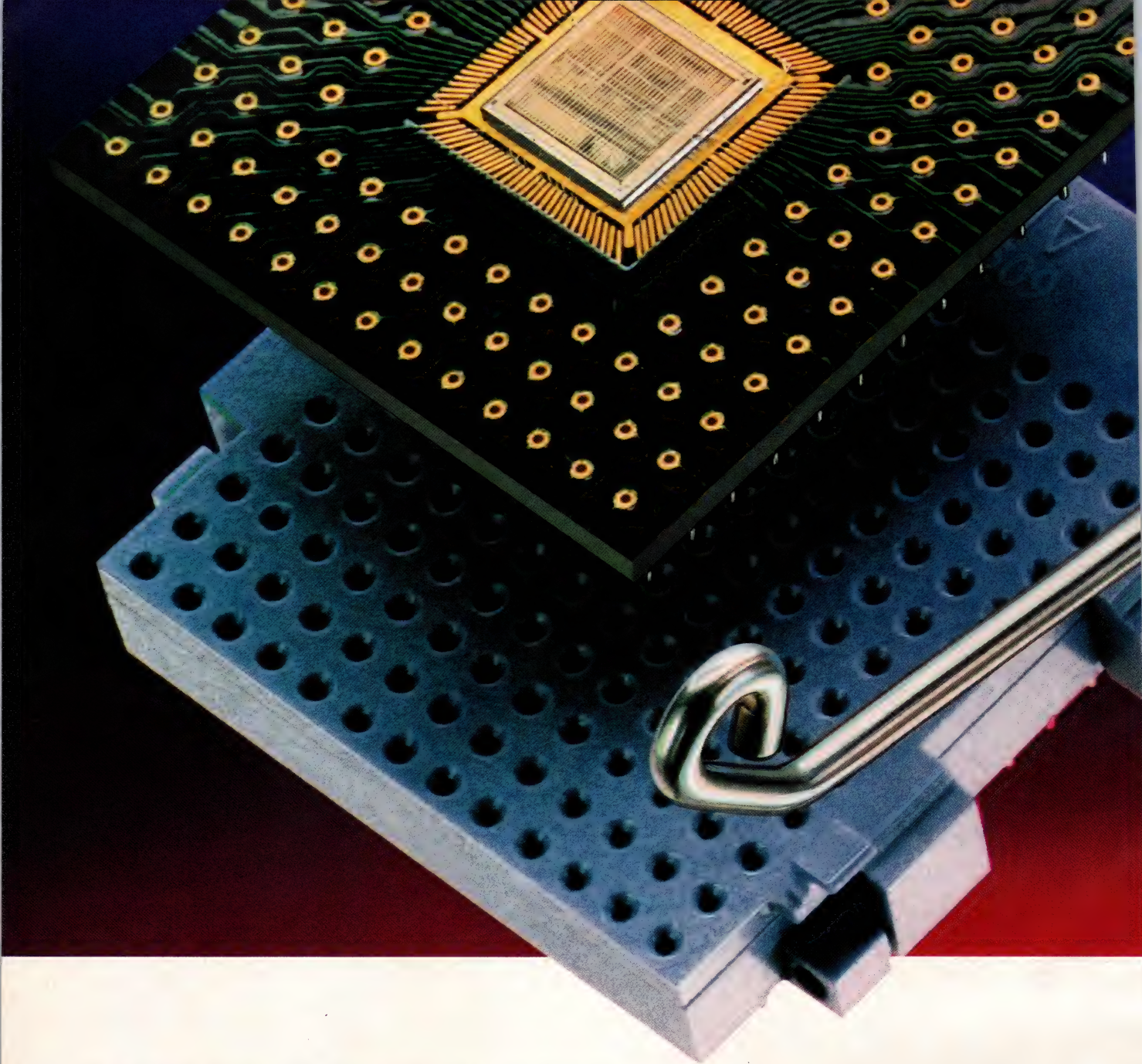


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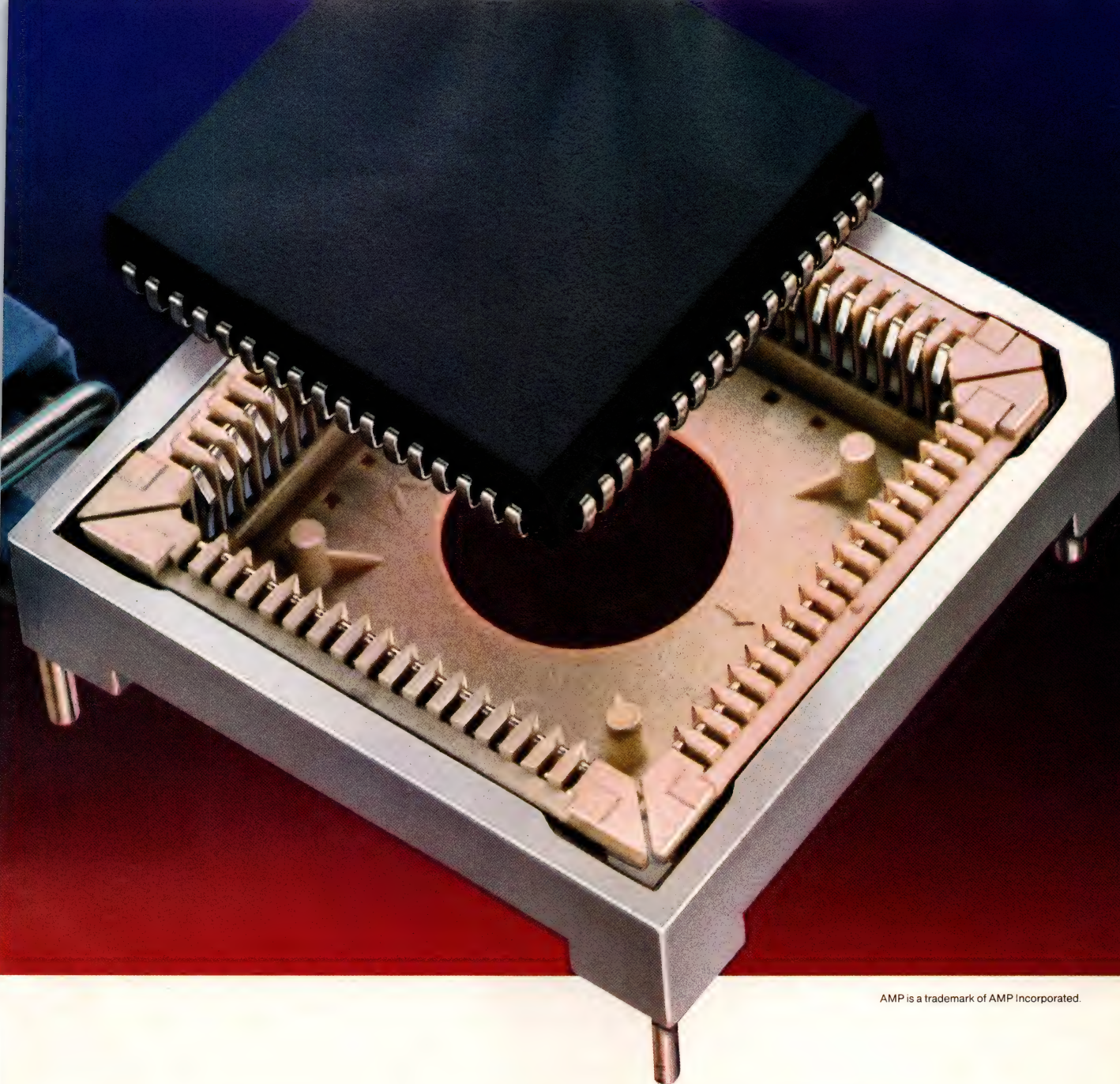
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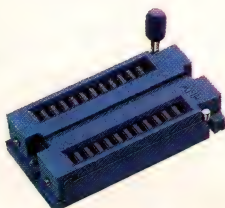
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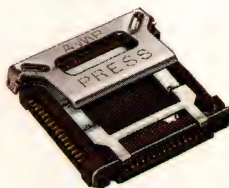
CIRCLE NO 93

AMP Interconnecting ideas

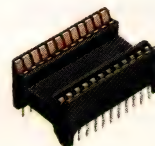
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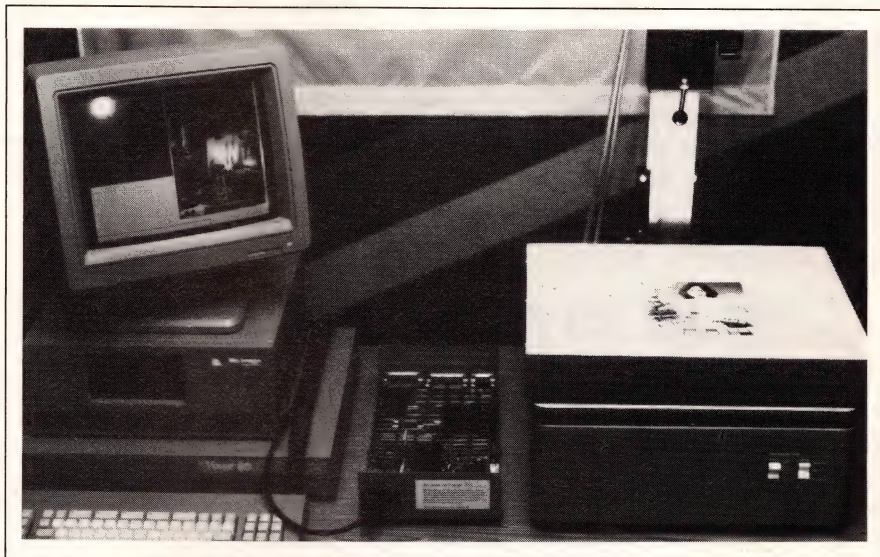
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WORKSTATIONS

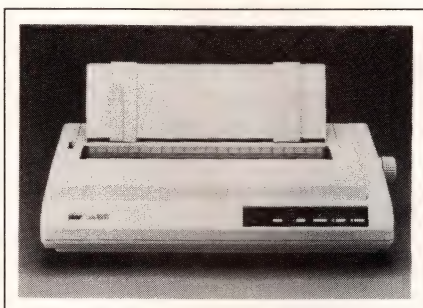
- *Utilize an 88100 RISC chip to deliver 14 to 17 VAX MIPS*
- *68020 μ P acts as graphics CPU, draws 450,000 2-D vectors/sec*

The XD88 family consists of two workstations that use Motorola's 88100 RISC chip. An application processor and a file server deliver 14 to 17 VAX MIPS; 34,000 Dhrystones; 16M single-precision Whetstones; and 7M to 12M flops. The system uses four 88200 cache memory-management units (expandable to eight) for a total of 64k bytes of cache. Standard configurations include 8M bytes of RAM (expandable to 176M bytes), a 156M-byte hard-disk drive, and a 150M-byte streaming-tape drive. Each unit has an independent 68020 μ P, acting as a graphics CPU, which provides redraw speeds of 450,000 2-D vectors/sec; 340,000 3-D vectors/sec; and 20,000 Gouraud shaded triangles/sec. The system displays 16.7M colors with 1280 × 1024-pixel resolu-

tion. The workstations also include X Window System version 11 and an option for stereoscopic displays. \$24,950 to \$34,950.

Tektronix Inc., Box 14689, Portland, OR 97214. Phone (800) 225-5434.

Circle No 379



PRINTERS

- *Eight resident fonts including Script and Courier*
- *Print at 300 cps in draft elite mode*

The XR-1500 Multi-Font and the XR-1000 Multi-Font are 9-wire dot-

matrix printers, featuring eight resident fonts: Courier, Script, Sans Serif, Letter G, TW-Light, Orator, Cinema, and OCR B. The units print at 300 cps in draft elite mode and 75 cps in near-letter-quality elite mode. When running in quiet mode, the printers operate at 51- and 50-dB noise levels, respectively. They each have a 32k-byte buffer, enabling them to store as many as 16 pages. An optional 128k-byte board expands the memory to 160k bytes. The printers differ only in carriage width and emulations. The XR-1500 is a 15-in. carriage model and emulates the Epson EX-1000 and IBM Proprinter IIXL printers. The XR-1000 is a 10-in. model and emulates the Epson EX-800 and the IBM Proprinter II printers. XR-1500, \$799; XR-1000, \$579; optional color-printing kit, \$50.

Star Micronics Inc., 200 Park Ave., Suite 3510, New York, NY 10166. Phone (212) 986-6770.

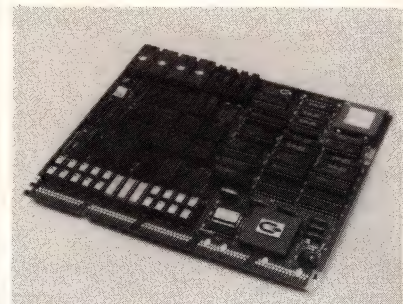
Circle No 380

DISK SUBSYSTEM

- Transfers data at 4M bytes/sec
- Controls as many as seven disk drives using DEC's MSCP

The DSB series consists of a disk-drive controller and a disk-storage subsystem for the VAX 8XXX and VAX 6XXX. The controller utilizes a 68020 μ P and a 64k-byte FIFO

buffer to transfer data at 4M bytes/sec. It controls as many as seven disk drives and occupies one slot in the VAXBI I/O Bus. The board operates with DEC's Mass Storage Control Protocol and has a SCSI port. In addition, the board has an RS-232C port for maintenance, diagnostic, and monitoring purposes.



The disk-storage subsystem has capacities ranging as high as 1G byte formatted. The subsystem is available in options that range from 19-in. rack-mountable units to fully configured cabinets. Rack-mountable drive and controller, \$22,500; 7-drive system in a 42-in. cabinet, \$114,500.

Clearpoint Research Corp., 99 South St, Hopkinton, MA 01748. Phone (508) 435-2000. FAX 508-435-6184.

Circle No 381

THE BATTERY FOR AUTOMATED PRODUCTION IS NOW IN PRODUCTION

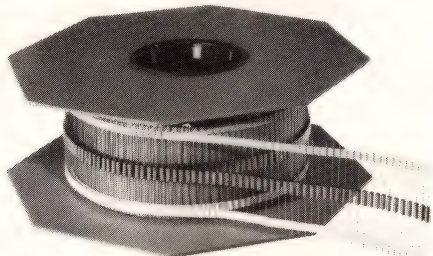


It's called the B-35 mPowerCell™. A CMOS backup battery that you can handle just like any other component. It is tape mounted for automatic insertion. It can be wave soldered. And, it withstands all normal flux cleaning and board drying procedures.

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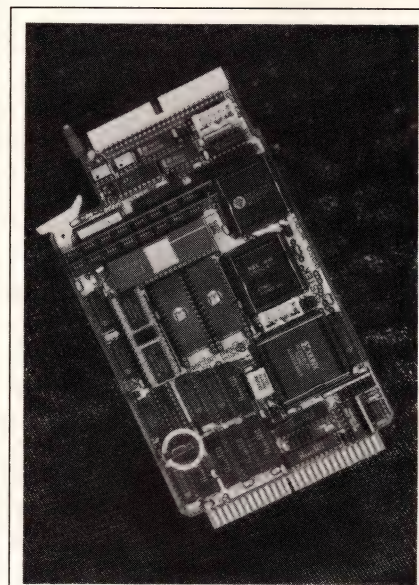
The B-35 has 35 milliamps-hours capacity. Enough for most CMOS backup applications. Although not tape mounted, higher capacity models (to 1 amp-hour) are available with all the other production advantages of the B-35.

For more information, call (301) 296-7000, ext. 304.



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CIRCLE NO 13



CPU BOARD

- Runs MS-DOS and has multiprocessing capability
- Has a V50 μ P and transfers both 16-bit and 8-bit data

The 8850 Multimaster single-board computer for the STD Bus runs MS-DOS and supports multiple boards on the bus in a multimaster configu-

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CIRCLE NO 97

ration. Among its features are a V50 μ P; 8-, 10-, or 12-MHz operating speed; two RS-232C ports and an RS-422/485 port; a parallel port; three DMA channels; three 16-bit timer/counters; 512k bytes of dynamic RAM; 32k bytes (expandable to 256k bytes) of EPROM; 128k bytes of battery-backed static

RAM; a socket for an 8087 coprocessor; and a battery-backed real-time clock/calendar. Transferring both 16 and 8-bit data and remaining compatible with the STD-8088 specification, the board is also compatible with 8-bit STD Bus boards and supports the 16-bit STD Bus standard. In parallel-processing ap-

plications, multiple boards can communicate through global memory located on the STD Bus. \$774 (OEM qty).

Systek, 1027 N Kellogg St, Kennewick, WA 99336. Phone (509) 735-1200.

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CIRCLE NO 14

MODEM MODULE

- Occupies 2.4×2.2 in. and communicates at 2400 bps
- Comes as a 44-pin DIP and has a DAA and RS232C interface

The MM2400-S 2400-bps modem in a 2.4×2.2 -in. module uses surface-mount technology and comes as a 44-pin DIP for installation on a pc board. The unit provides full-duplex communications over a twisted-pair telephone network. Equipped with a data-access arrangement and an RS-232C interface, the unit supports both synchronous and asynchronous communications. The unit is compatible with the Hayes extended AT command set and can operate at 2400, 1200, and 0 to 300 bps. The modem conforms to CCITT V.22 bis, V.22, and V.21 standards, as well as Bell 212A and 103 standards. In addition, the unit contains transmit and receive filters, automatic equalization, and modulation/demodulation. Supporting both DTMF and pulse dialing, it also has telephone-call progress monitoring. \$130 (1000).

Micro Electronic Technologies Inc., 35 South St, Hopkinton, MA 01748. Phone (508) 435-9057. FAX 508-435-6481.

Circle No 383

INTERFACE ADAPTER

- Connects DTEs or DCEs with RS-232C, RS-422, or CCITT V.35 ports
- Has six status LEDs for each of its ports

The TriX-1 adapter connects incompatible interfaces. It has three line connectors on its rear panel: a 25-

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pin D connector as an RS-232C port, a 37-pin D connector as an RS-422 port, and a 34-pin M-block connector as a CCITT V.35 port. The unit permits data terminal equipment and data communications equipment with incompatible ports to connect with other DTE and DCE units. A front-panel switch on each connector determines whether the port is a DTE or a DCE unit. The RS-232C interface also has a second switch that can connect pin 15 (transmit timing, DCE source) of the RS-232C port to either pin 17 (receive timing) or to pin 24 (transmit timing, DTE source). Six front-panel LEDs for each of the interfaces indicate active status for the following signals: send data, receive data, send timing, receive timing, request to send/data terminal ready, and clear to send/data set ready. \$450. Delivery, five weeks ARO.

Integrated Communications Inc., Box 780, Germantown, MD 20874. Phone (301) 948-4133. FAX 301-972-3698.

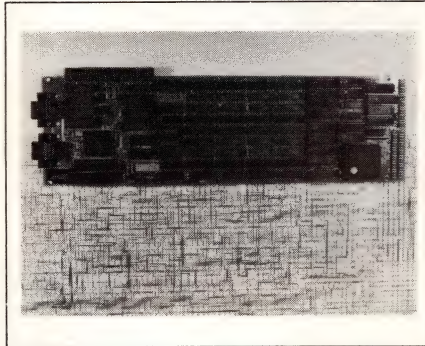
Circle No 384

VIDEO CONTROLLER

- Uses the VLSI 86010 RISC μ P
- Displays $1024 \times 768 \times 4$ -bit pixels with 16.8M colors

The VectorScan RISC is a graphics coprocessor board for the IBM PC, PC/XT, PC/AT, and compatible computers that uses a VLSI 86C010 32-bit RISC μ P as a video controller. The CPU's instruction set is similar to that for the TMS4010 but the CPU fetches a 32-bit instruction

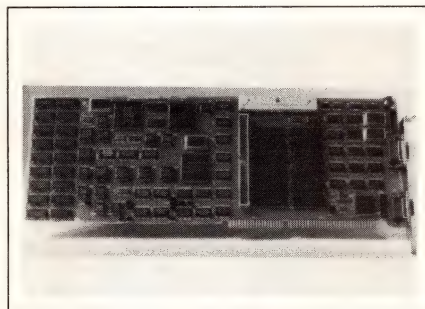
in a single cycle. The controller provides 4-bit displays measuring 1024×768 pixels or 640×480 pixels and 8-bit displays with 800×600 pixels, with 16.8M colors at its analog output or 64 TTL colors at its digital output. The host communicates with the board through interrupts, DMA, or programmed I/O instructions. The unit draws 600,000 pixels/sec and more than 13,000



characters/sec. A video-switch feature lets you connect a DOS-compatible video card through the controller board to a monitor. \$695.

Applied Data Systems Inc., 409A E Preston St, Baltimore, MD 21202. Phone (301) 576-0335.

Circle No 385



IMAGING BOARD

- Contains a TMS34010 and a TMS320C25 μ P
- Has 2M bytes of main memory and performs bitblt in hardware

The Gemini, an image-processing board for the IBM PC/AT and compatible computers, consists of a TMS34010 graphics system processor (GSP) and a TMS320C25 digital signal processor (DSP). Because the DSP has its own local bus and mem-

ory system, it can operate independently of the GSP. The board also contains multiple look-up tables, 2M bytes of main memory, and a 256k-byte display buffer with an additional 128k bytes for graphics overlay. The board performs bitblt operations in hardware that can transfer image data into the display buffer at 5M bytes/sec. In addition, the board has 2M bytes of annotation memory, which permits text and graphics overlays without loss of image data. The board comes with IWindows software, which supports multiple concurrent tasks. The software can overlap multiple images using windows. Board and software, from \$3995.

Imagesystems Inc., 7504 134th Ave SE, Renton, WA 98056. Phone (206) 255-0899.

Circle No 386

SCSI CONTROLLER

- Has as much as 1M byte of cache RAM
- Includes 10-MHz 80188 μ P to control seven SCSI disk drives

The LDP-CACHE SCSI disk-drive controller for the IBM PC, PC/XT, PC/AT, and compatible computers has a 10-MHz 80188 μ P and from 256k bytes to 1M byte of cache memory. The board keeps the most recently accessed data in local RAM, thus reducing disk seek times and latencies. The board also reads an entire track into its local RAM each time it accesses a track, making other sectors on the track immediately available. Further, the board queues write requests in its RAM, and its 80188 CPU performs write operations by sequencing through pending writes in order of closest access on the drive. The intelligent interface transfers data at 4M bytes/sec and controls as many as seven SCSI disk drives. You can set four port addresses with jumpers from 000H to 3FFH. The board's support of a 1:1 interleave ratio on a hard disk allows the board

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Lomas Data Products Inc., 182 Cedar Hill St, Marlboro, MA 01752. Phone (508) 460-0333.

Circle No 387

HANDHELD TERMINAL

- Features an LCD with four 20-character lines
- Lets you develop code in C language on IBM PC/AT

The HT/1120 user-programmable handheld terminal allows users to develop code in C language on an IBM PC/AT or compatible computer. Users then cross-compile the code to HD6303 machine instructions with a suitable compiler, such as the Archimedes Software C-6301 cross-compiler, and download the code to the terminal. The unit comes with either an RS-232C, RS-422, current loop, or TTL inter-

faces. Providing 256k bytes of surface-mount RAM, the unit comes with alkaline batteries for completely portable operations. In addition, the LCD has four 20-character lines, and the 32-key alphanumeric keyboard provides user-selectable options. The unit comes with a 2-year warranty. \$1000 (OEM qty). Delivery, eight weeks ARO.

Termiflex Corp., 316 Daniel Webster Hwy, Merrimack, NH 03054. Phone (603) 424-3700.

Circle No 388

PRINTER ADAPTER

- Compatible with Centronics printers
 - Printing of paint programs on color or black-and-white printers
- The NB-PRL, a Centronics parallel interface board for Macintosh II computers, provides the standard Centronics handshake signals that

permit the host to communicate with a compatible printer or plotter. The board can transfer data at a maximum speed of 150k bytes/sec. Color pictures drawn by paint programs can print in color or black and white. The unit also permits Macintosh word-processing programs to be printed on printers with compatible interfaces. The digital interface utilizes an AMD 8255 programmable peripheral interface. In addition, the board contains a configuration ROM, an address decoder, and NuBus control circuitry. The digital I/O interface takes place through a 25-pin D sub-female connector. \$245; 2-meter Centronics cable, \$45.

National Instruments Corp., 12109 Technology Blvd, Austin, TX 78727. Phone (800) 433-3488; in TX, (512) 794-0100. FAX 512-250-9319. TLX 756737.

Circle No 389



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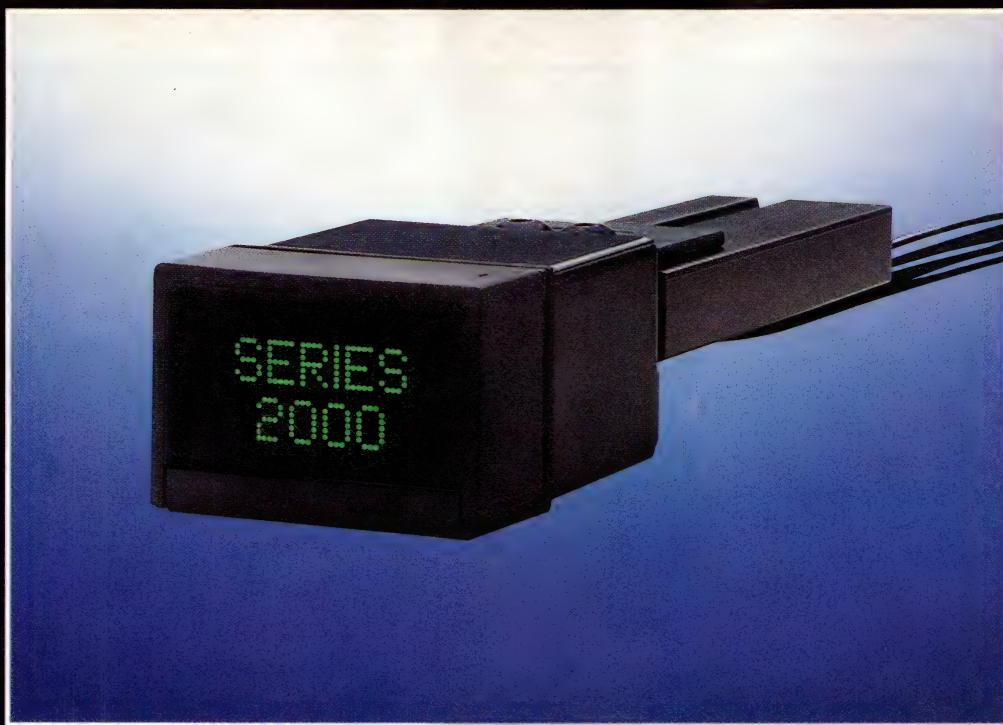


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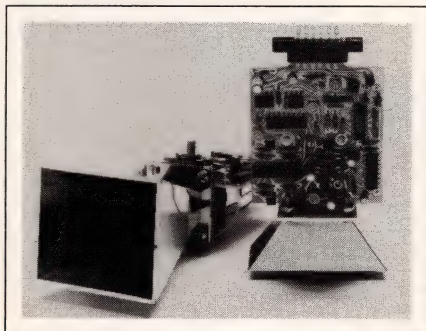
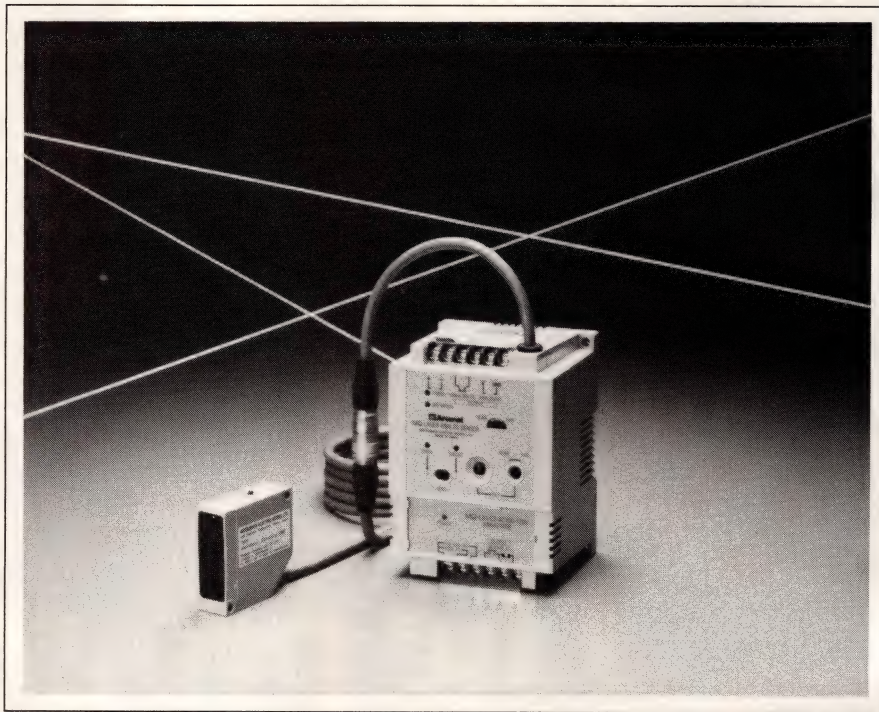
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- Offer digital and analog outputs

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Aromat Corp., Industrial Products Div, 629 Central Ave, New Providence, NJ 07974. Phone (201) 464-3550.

Circle No 365



SENSOR KIT

- Comes with two antennas
- Motion-sensing module meets FCC regulations

The MSM 10200 microwave, non-contact, motion-sensor evaluation kit is furnished with two horn antennas. The broad-beam antenna has a sensing range of 50 ft max and is suited for large targets. The narrow-beam unit is useful for small objects and has a 150-ft max sensing range. A sensing module, which operates in a transmit/receive mode, an application note on sensor interfacing, and pc-board-mountable signal-conditioning electronics com-

plete the kit. The sensor module meets FCC regulations for frequency, output power, stability, and emissions. It operates from 10 to 26V dc inputs and draws only 10 mA. The signal-conditioning circuitry contains the power supply, amplifiers, comparator, and an output switch, which drives the oscillator and converts the detected output to either a switch closure output or an analog output. \$195.

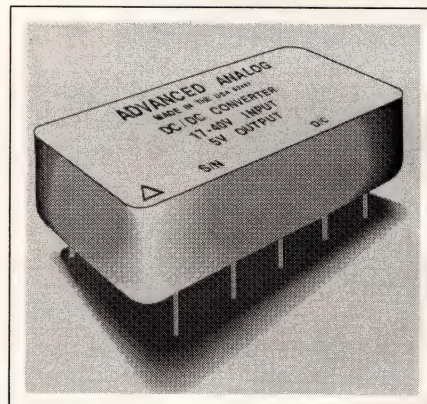
Alpha Industries, 20 Sylvan Rd, Woburn, MA 01801. Phone (617) 935-5150. FAX 617-935-4939.

Circle No 366

DC/DC CONVERTERS

- Offer 84% efficiency
- Meet military specifications

AHE2800 Series dc/dc converters are available with single or dual outputs that have 15 or 20W output ratings. All units meet the requirements of MIL-STD-704D. Switching frequency is 250 kHz, and efficiencies range from 78 to 84%. Line



and load regulation measures $\pm 0.5\%$, and output ripple is 60 mV max. Units are available with 5V (AHE2805), 12 and $\pm 12V$ (AHE2812), and 15 or $\pm 15V$ (AHE2815) outputs. Models operate over -55 to $+85^\circ C$, -55 to $+105^\circ C$, or -55 to $+125^\circ C$. Units screened to MIL-STD-883C are also available. \$299 to \$320 (100) for -55 to $+85^\circ C$ converters.

Advanced Analog, 2270 Martin Ave, Santa Clara, CA 95050. Phone (408) 988-4930. FAX 408-988-2702.

Circle No 367

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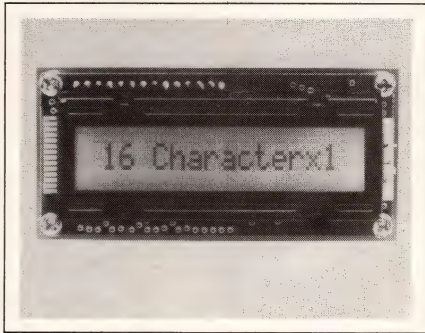
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DISPLAY MODULE

- Operates from a 5V supply
- Features a direct CPU interface

The AND673-JO is a 16-character x 1-line liquid-crystal-display module that features built-in LED backlighting. The unit operates from a 5V supply and features 11 wide-angle yellow dies, which provide a display that's suited for use at night. The display's onboard LCD controller, display RAM, and character generator combine to provide a direct display interface to

either a 4- or 8-bit CPU. The unit features 3.1 x 5.76-mm characters, which are displayed in a 64.5 x 13.8-mm viewing area. The built-in backlight draws 110 mA from a 4V supply. \$25 (100).

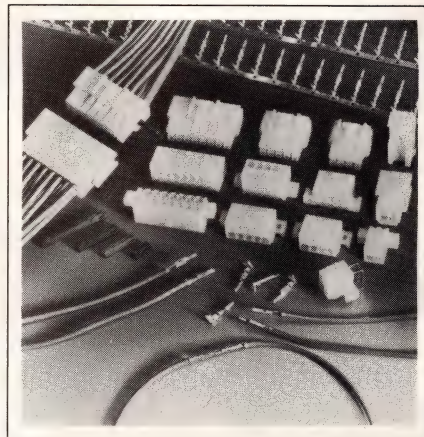
AND, 770 Airport Blvd, Burlingame, CA 94010. Phone (415) 347-9916. FAX 415-340-1670.

Circle No 368

POWER CONNECTORS

- Feature secondary locks
- Can handle 9A per contact

Mini-Fit TPA power connectors feature secondary locks in the form of red-colored keys, which are inserted into the housing to ensure that the terminals within are correctly and permanently seated. Connectors are available with 2 to 16 positions located on dual rows with a 0.165 x 0.217-in. grid. The contacts can handle 9A at 250V.



Both halves of the connector are fully shrouded to protect the contacts from damage and shorting. The female crimp contact is formed into a box shape. Dimples on two sides of the box provide four contact points with the male terminal. The UL-recognized and CSA-certified connectors are available with 94V-2- and 94V-0-rated housings. Brass

Text continued on pg 189



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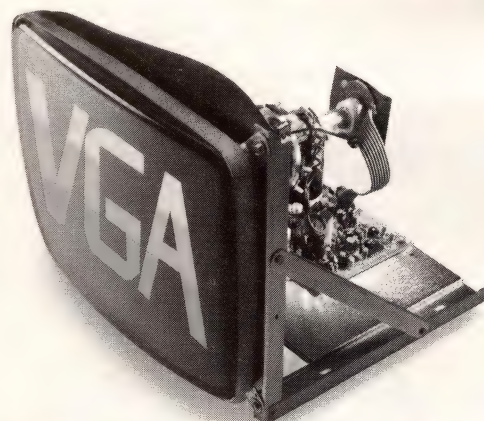
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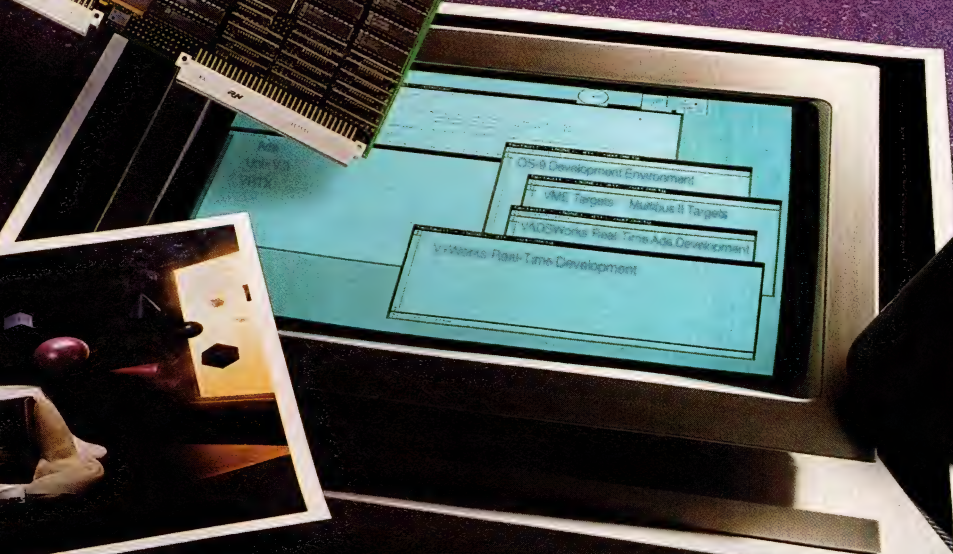
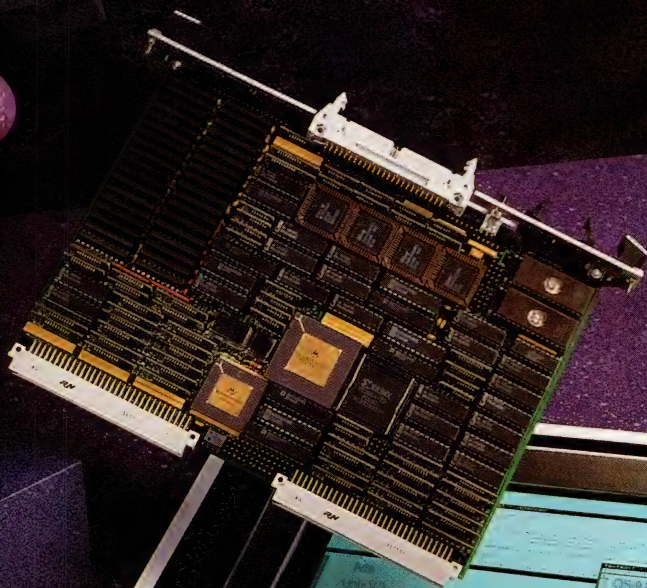
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Imagine a memory that expands to 256K—and with four channels, one MegaSample. A unique, removable 44 Megabyte hard disk giving you *ten times* faster data recall and transfer. Time-saving PC interface. MS-DOS, disk downloadable sequences and programs you can customize. Unmatched calculation speed. Easy data archiving. Even four models offering your choice of speed and resolution.

That's the new Nicolet 400 Series.
Power. Speed. Flexibility.
Convenience. To see what you've
been missing in *waveform acquisition*,
call or write today.

Nicolet Test Instruments Division

5225-2 Verona Road, Madison, WI 53711, 608/273-5008 or 800/356-3090

Nicolet

INSTRUMENTS OF DISCOVERY

CIRCLE NO 106

or phosphor-bronze contacts are available with either select-gold or tin platings. \$0.06/mated line for a 10-position model. Delivery, four to six weeks ARO.

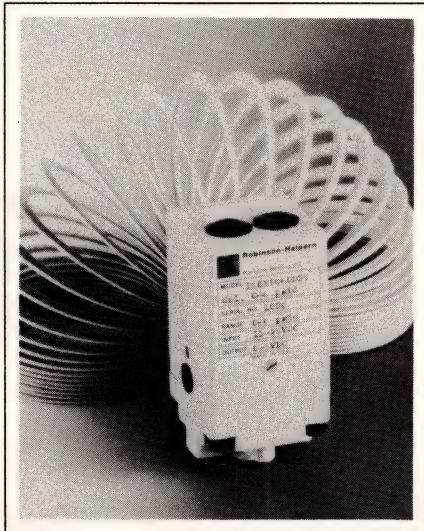
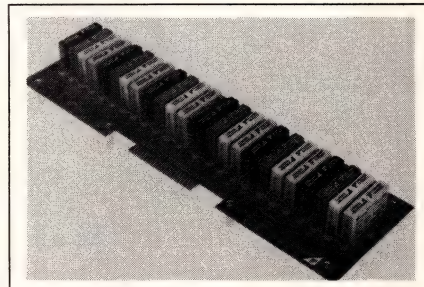
Molex Inc., 2222 Wellington Ct, Lisle, IL 60532. Phone (312) 969-4550. TLX 254069.

Circle No 369

I/O RACK

- *Saves real estate*
- *Comes with pull-up resistors and load fuses*

Measuring only 3.75×13 in., the Model PB-24SM digital I/O rack occupies 42% less space than standard PB-24 racks. The unit will accept as many as 24 of the manufacturer's



TRANSMITTER

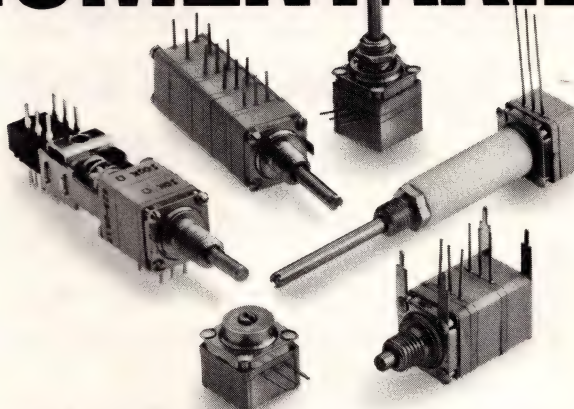
- *Measures liquid or gas pressures*
- *Features a 6.5 turn-down ratio*

Model 150 differential transmitter eliminates the need for custom pressure sensors. The unit measures gauge, differential, or absolute pressures of liquids or gases. Models are available with measurement ranges of 1.5 to 300 psi with accuracies of ± 0.5 . The operating span can be compressed from 100 to 15% of the rated range, equivalent to a 6.5 turn-down ratio. You can also compress zero by as much as 85%; zero and span adjustments are externally accessible. The transmitter's aluminum housing carries a NEMA 1 rating. An internal regulator features polarity reversal protection and permits operation from an unregulated power source. \$325.

Robinson-Halpern Products, 1 Apollo Rd, Plymouth Meeting, PA 19462. Phone (215) 825-9200. FAX 215-834-1917.

Circle No 370

MODULAR POTS MOMENTARILY!



The individual components of our $\frac{1}{2}$ -inch-square conductive plastic and cermet potentiometers are stackable and interchangeable. Easily. Quickly. And economically.

They meet MIL-R-94 and MIL-STD-202 standards. Customized options include terminal variations, detents, and various shaft and bushing configurations. And power ratings are 0.5 and 1.0 watts.

Each pot can be combined with SPST or SPDT rotary switch modules, SPDT push-pull or momentary switches and in multiple sections of as many as 8 modules.

We guarantee same day shipping on all standard orders received before noon. Don't delay. For complete details call or write Doug Tarr, Product Manager at CLAROSTAT, One Washington Street, P.O. Box 1507, Dover, NH 03820-1507. Telephone (603) 742-1120. TLX VIA MCI 671 3344. Fax (603) 742-0481. To Order Call **Toll-Free 1-800-872-0042**.

WHY WAIT?



ALL POWER SUPPLY ROADS LEAD TO

SCR ϕ CONTROL
SWITCH MODE

ARC
LAMPS

BURN-IN

ELECTRO
PLATING

LASERS

ELECTRO
MAGNETS
AND
BEAM
BENDING

**TO SWITCH OR NOT TO SWITCH...
NEED NOT BE THE QUESTION...
WE'VE GOT IT ALL!!!**

- **SCR PHASE CONTROL** There are 101 catalog models to choose from ... in 1 ϕ or 3 ϕ ... 250W to 100,000W ... 6.0 vdc to 600 vdc ... 0.9A to 3,000A ... remote sense/programmable ... 1/2 rack to floor mounts.
- **DC SWITCH MODE** With 32 catalog models ... in 1 ϕ & 3 ϕ ... 250W to 6,000W ... 7.5 vdc to 380 vdc ... 0.5A to 600A ... remote sense/programmable ... shoe box or rack mount.

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application assistance call
1-800-631-4298



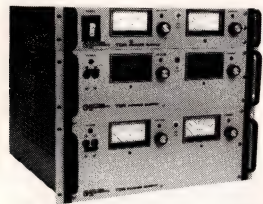
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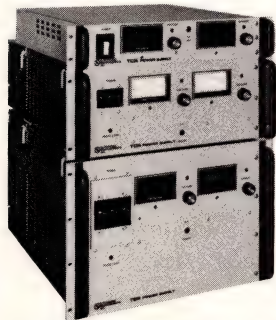
SCR REGULATED DC POWER SUPPLIES



SINGLE PHASE TCR

- 4 power levels 600 W - 1,000 W - 1,800 W - 2,800 W

- DC outputs variable over full range of 0 to 7.5 V DC through 0 to 2,500 V DC
- Regulated and metered (V and A)
- CV/CC with automatic crossover
- Fully programmable and remote sense
- Complies with VDE 875-N and VDE 871-A
- 5-year warranty



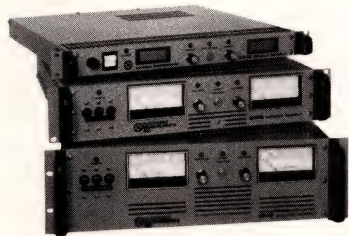
THREE PHASE TCR

- 3 power ranges 2,500 W - 5,000 W - 10,000 W
- DC outputs variable over range

from 0 to 6 V DC through 0 to 600 V DC

- Regulated and metered (V and A)
- CV/CC with automatic crossover
- Complies with VDE 875-N and VDE 871-A
- 5-year warranty

EMS HIGH FREQUENCY SWITCHING DC POWER SUPPLY



- 48 models 600 W to 1,000 W to 2,500 W to 10,000 W
- Voltages from 7.5 V DC through 1,000 V DC
- High density packaging — up to 3.1 W/cubic inches at 5 kW
- Regulated and metered (V and A)
- Fully programmable and remote sense
- CV/CC with automatic crossover
- 5-year warranty
- U/L recognized

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405 Essex Rd., Neptune, NJ 07753, Dept. EM
TOLL FREE: 800-631-4298

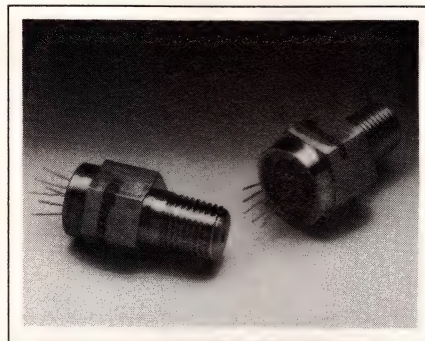
CIRCLE NO 18

COMPONENTS & POWER SUPPLIES

SM Series I/O modules. Standard rack features include LED indicators, 3.3-k Ω pull-up resistors, load fuses, field wiring, power-supply barriers, and a gold-plated card-edge connector. Options include detachable barriers, vertical or horizontal header connectors, and a hold-down bar, which is useful in harsh environments. \$102.

Gordos, 1000 N Second St, Rogers, AR 72756. Phone (800) 643-3500.

Circle No 371



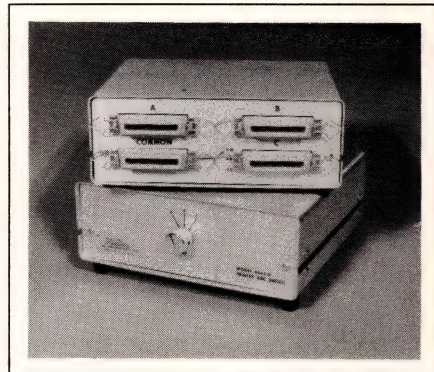
PRESSURE SENSORS

- Available with integral temperature compensation
- Feature a $\pm 0.25\%$ accuracy

Models 90 and 93 solid-state pressure sensors have a 5 to 3000-psi gauge or absolute measurement range and a $\pm 0.25\%$ accuracy. All exposed surfaces of the sensors are made from 316 stainless steel, which allows the units to accommodate most harsh media. With a 1.5-mA excitation, output span is typically 100 mV. With Model 90 devices, you can calibrate and compensate the sensors for 0 to 50°C operation using only three external resistors, which are included with each device. Model 93 units are internally calibrated and compensated for operation over 0 to 50°C. Model 90, from \$98; Model 93, from \$108. Delivery, stock to six weeks ARO.

IC Sensors Inc., 1701 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1800.

Circle No 372



INTERFACE SWITCH

- Lets a computer select from three printers

- Handles any parallel interface

In minicomputer applications, Model 8863-D 3-way transfer switch allows the computer to select among three printers. In multiple μ C installations, you can use the device to switch a single printer to support three μ Cs equipped with a parallel interface. Because all conductors at the 36-pin connector are switched, the 8863-D will accommodate any parallel-interfaced printers. You can easily make all interface connections through the four 36-pin connectors (labeled A, B, C, and Common) on the switch's rear panel. The front-panel selector switch routes the data from the Common connector to the appropriate device connector. \$220.

Electro Standards Laboratory Inc., Box 9144, Providence, RI 02940. Phone (401) 943-1164.

Circle No 373

POWER MOSFETs

- Operate with 5V gate level
- Feature 24W dissipation

The IRL110 and 120 MOSFETs require only a 5V gate signal for full turn-on. The 110 has a 3.6A drain current rating and an on-resistance of 0.58 Ω . The 120 has a 4A drain-current capability and a 0.35 Ω on-resistance. The 110 and 120 have a peak diode recovery of 5.5V/nsec; repetitive avalanche energy is 1.8 mJ for the 110 and 2.4 mJ for the 120. Maximum power dissipation

ratings are 18 and 24W for the 110 and 120, respectively. IRLF110, \$10.71; IRLF120, \$11.93 (1000). Delivery, eight to 10 weeks ARO.

International Rectifier, 233 Kansas St, El Segundo, CA 90245. Phone (213) 607-8899.

Circle No 374

TRANSDUCERS

- Accommodate harsh environments
- Have a 50-mV output span

Model P5021 pressure transducers incorporate a 300 Series stainless-steel chamber, which allows the units to handle a variety of corro-



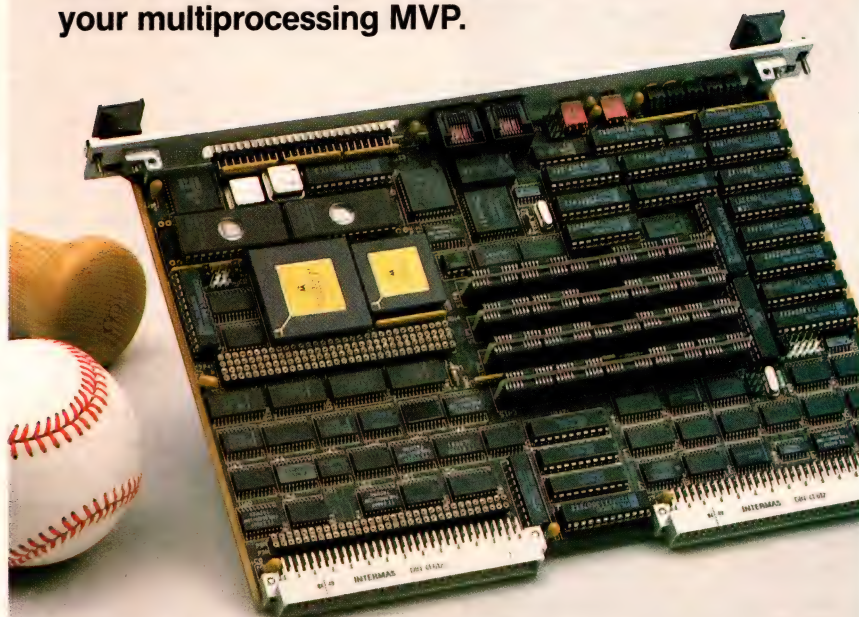
sive liquids and gases. The transducers provide vented-gauge pressure measurements in full-scale ranges of 15 to 5000 psi. The devices operate from a 5V supply and provide a 50 ± 1 -mV dc full-range output. Combined linearity, hysteresis, and repeatability is $\pm 1\%$ at full-scale output. All transducers are fully calibrated and compensated to ensure unit interchangeability. From \$130.

Schaevitz Engineering, 7905 N Rte 130, Pennsauken, NJ 08110. Phone (609) 662-8000. FAX 609-662-6281.

Circle No 375

Team player

Make Mizar's dual-ported 68030 CPU your multiprocessing MVP.



You're sure to score with Mizar's MZ 7130, the VME microcomputer with major league features. Combining 68030 power and true dual-ported memory, the MZ 7130 wins the multiprocessing pennant. All for a price that won't send you into the dugout.

Rely on the MZ 7130 for functionality: a 68030 MPU at up to 25 MHz, four MB of dual-ported DRAM with parity, 16K cache, up to one MB of EPROM, two RS-232 serial ports, SCSI, mailbox interrupts, and time-of-day clock.

Draft from options such as a 68882 FPP, up to one MB of SRAM, a VSB interface, and Ethernet™.

Build your real-time application around Mizar's team player, the MZ 7130. Call today. **1-800-635-0200**.

Mizar. The shortest distance between concept and reality.

MIZAR

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PROCESS METER

- Features a built-in power supply
- Provides 3½-digit output span

Model 205-E digital process meter features an internal power supply rated for 24V at 20 mA or 10V at 30 mA. You can use this supply to power 2- or 4-wire transmitters and other active sources. The unit provides 3½ digits of display span. Zero and span adjustments are made from the front panel. Full-scale signal ranges of 4- to 20 mA, 0 to 0.2V, 1 to 5V, 0 to 10V, and 0 to 100V are jumper-selectable. The true-differential input has 56 dB of normal-mode noise rejection. Screw-clamp cable connectors, which comply with VDE and UL requirements, are standard for power, signal, and excitation output. The meter housing is made of

COMPONENTS & POWER SUPPLIES

94V-0 UL-rated polycarbonate.
From \$149.

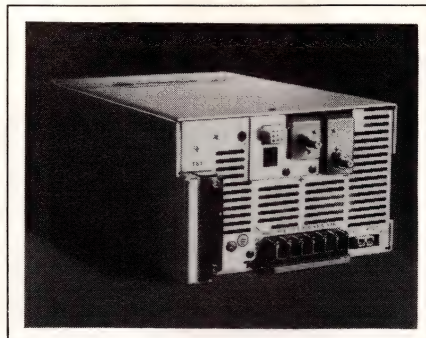
Newport Electronics Inc., 2229 S
Yale St, Santa Ana, CA 92704.
Phone (714) 540-4914. FAX 714-
546-3022.

Circle No 376

BACKUP SUPPLIES

- Operate with ac or dc inputs
- Feature isolated outputs

BB Series 750W switching power supplies operate from 115/230V ac inputs or a 48V sealed lead-acid battery. As many as four outputs with voltages of 2 to 48V are available. All outputs are electrically isolated and can be connected for either positive or negative output polarities. The supply normally operates from the ac line. When the ac fails, the device draws power from the battery through a switching up-converter to keep the main converter

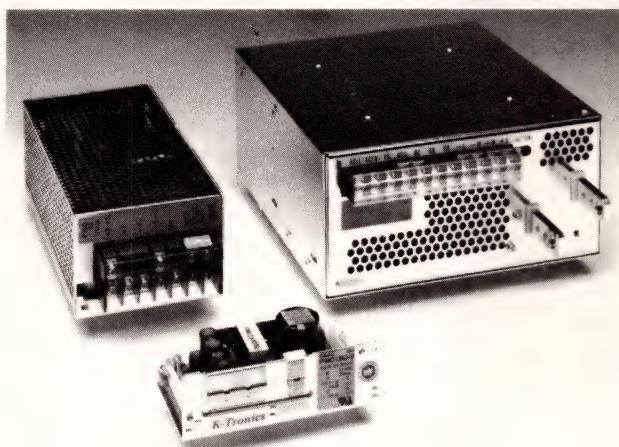


operational. Supply features include remote inhibit, remote main-output margining, ac power fault detection, overvoltage protection, and main-output out-of-tolerance protection. The units are recognized by UL, approved by CSA, and comply with VDE safety standards. From \$1470.

Unipower Corp., 2981 Gateway Dr, Pompano Beach, FL 33069.
Phone (305) 974-2442. FAX 305-971-1837.

Circle No 377

ELCO P Series Worldwide Input Power Supplies



- o 15 watt to 1500 watt models, single output
- o PMC versions; multiple outputs; 15 watts up to 100 watts
- o UL, CSA & TUV approved, or pending
- o High Efficiency—up to 4.2 watts per cubic inch on P1500
- o Molex or screw terminals (most models)
- o Meets FCC & VDE EMI requirements; high MTBF
- o Smaller than industry standard footprints

For information contact:
K-Tronics, a division of K.T. Electronics.
341 Cobalt Way, #206, Sunnyvale, CA 94086
Phone 800 888-ELCO; FAX 408 732-5049

CIRCLE NO 20

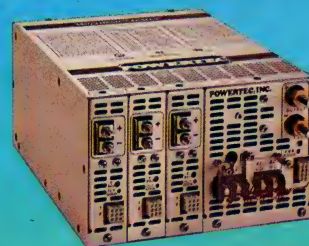
ELCO

NEW! SWITCHMODE POWER SUPPLIES FROM STOCK

- 2 to 48 VDC Outputs
- Automatic Current Sharing On All Outputs
- N+1 Capabilities



MULTIPLE OUTPUT



- 350 to 1500 Watts
- 3 to 15 Outputs

SINGLE OUTPUT



- 400 to 3000 Watts in 5" x 8" Standard Package
- 155,000 Hrs. Demonstrated MTBF

Hot Plug-In FAULT TOLERANT (N+1) POWER SYSTEMS



- Two to Six Supplies
- Expandable, 300 to 1800 Watts
- Internal Isolation Diodes (Option)

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The Power in Power Supplies

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CIRCLE NO 22

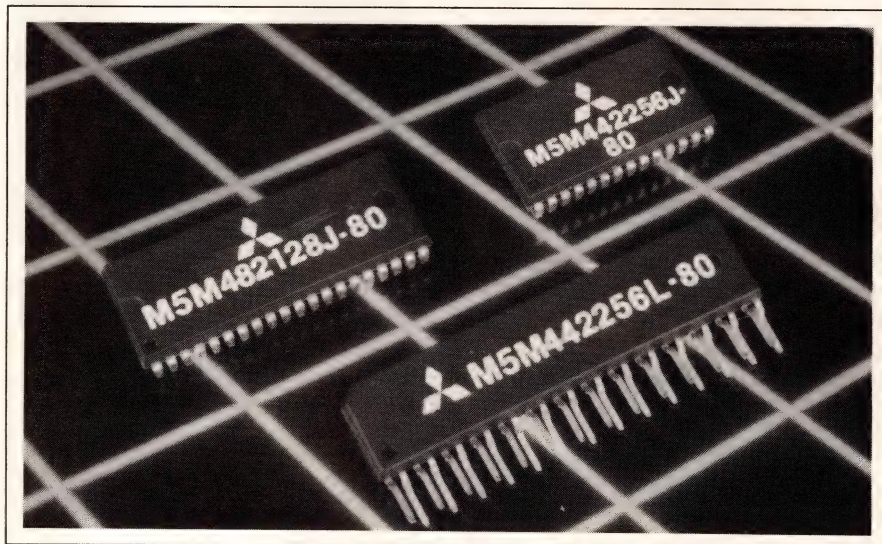
NEW PRODUCTS

INTEGRATED CIRCUITS

1M-BIT VIDEO RAM

- Available in two configurations
- Access times as low as 80 nsec

Organized in two different configurations, these 1M-bit video RAMs are available with maximum access-time ratings of 80, 100, and 120 nsec. The M5M482128 dual-port dynamic RAM has a 128k $\times$ 8-bit dynamic RAM parallel-access memory port combined with a 256 $\times$ 8-bit serial-access memory (SAM) port. The M5M442256 has a 256k $\times$ 4-bit DRAM port combined with a 512 $\times$ 4-bit SAM port. The parallel port acts as a standard DRAM accessed by a μ P or video controller. The bidirectional SAM port, which allows high-speed conversion of parallel data to a serial bit stream or vice versa, shifts the DRAM data out to a RAM DAC for display on a CRT. The inclusion of both ports

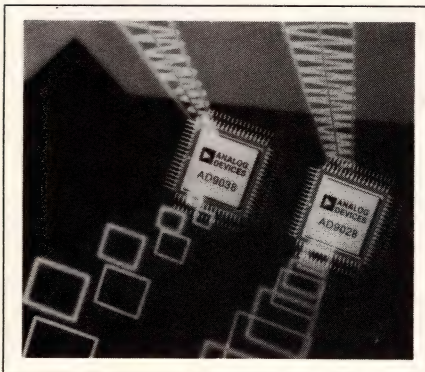


in a single device improves performance and reduces external logic requirements. Depending on type, package options include 40-pin and 28-pin SOJ packages, and 28-pin ZIPs. 80-nsec versions, \$57.50 and

\$62 (100).

Mitsubishi Electronics America Inc., 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900.

Circle No 390



8-BIT ADCs

- Critical ac specs are guaranteed
- Converts at 300M samples/sec

Producing 8-bit A/D conversions as fast as 300M samples/sec, the AD9028 and AD9038 have guaranteed specs for all critical ac parameters. Providing identical performance, the flash converters offer a choice of digital interfacing rates. The AD9028 uses a single parallel ECL-compatible output latch, and the AD9038 provides a 1:2 demultiplexed output via two latches that interface to slower logic. Both de-

vices feature a 250-MHz analog bandwidth, a 36-dB S/N ratio for 92-MHz inputs, and a 47-dB S/N ratio for 9.3-MHz inputs. The maximum differential and integral nonlinearities are $\frac{3}{4}$ LSB (J grade) and 1 LSB (K grade) with guaranteed 8-bit no-missing-code performance. The analog input spans a signal range of 0 to -2V, and the input capacitance is 17 pF. Power consumption is <2.1W typ from a -5.2V supply. From \$185 (100).

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 935-5565.

Circle No 391

MATH COPROCESSOR

- Works with Intel 80486 μ P
- Plugs into a socket on the system board

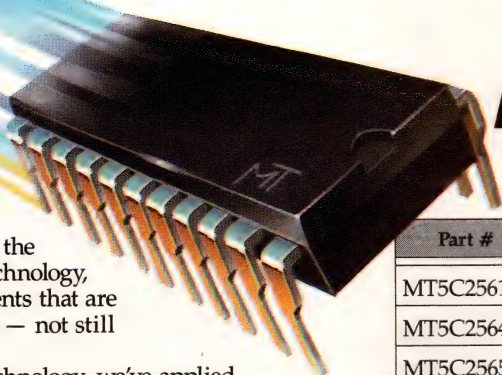
The Abacus 4167 is a floating-point coprocessor for the Intel 80486 μ P that completes math operations 5 to 6 times faster than the 486's on-

chip floating-point unit. The 4167 plugs into a socket on the system board of 486-based computers, enabling them to run numerically intensive applications 2 to 3 times faster than systems with the 486 alone. Using the 4167, a 486-based PC running at 25 MHz can deliver 17M Whetstones of single-precision performance, compared with 7M Whetstones delivered by the 486 alone. All existing applications that support the company's Abacus 3167 for 386-based computers automatically support the 4167. The Abacus 4167 has a 64-bit floating-point data path, which includes an ALU, a multiplier, and a divide/square-root unit. Packaged in a 142-pin pin-grid array, the 4167 is available in sample quantities now. Limited production quantities will be available in December 1989. \$565 (1000).

Weitek Corp., 1060 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 738-8400.

Circle No 392

SUPER FAST SRAMS, PRODUCTION PROVEN.



**Available Now! 256K 25ns
64K 15ns/16K 15ns**

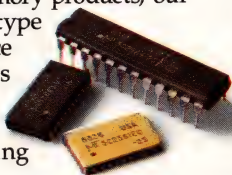
When you work at the leading edge of technology, you need components that are production proven — not still in development.

At Micron Technology, we've applied the same state-of-the-art design and process technology used for our high quality DRAMs in development of our Fast Static RAMs. The result — an incredible 25ns 256K and 15ns 64K and 16K, plus a full line of other super fast parts. And we're not just sampling product, we've been shipping production volumes for over a year.

A wide variety of packages, densities and organizations are offered to meet all your application needs. And like all Micron memory products, our Fast SRAMs are backed by the type of strong sales, customer service and technical support that keeps you on the leading edge.

So get the Super Fast SRAMs you need now by calling us at 1-208-386-3900.

Micron. Working to improve your memory.



Part #	Organization	Speed*	Packages
MT5C2561	256K X 1	25ns	PDIP, CDIP, SOJ, LCC
MT5C2564	64K X 4	25ns	PDIP, CDIP, SOJ, LCC
MT5C2565	64K X 4 $\overline{\text{OE}}$	25ns	PDIP, CDIP, SOJ, LCC
MT5C2568	32K X 8	25ns	PDIP, CDIP, SOJ, LCC
MT5C6401	64K X 1	15ns	PDIP, CDIP, SOJ
MT5C6404	16K X 4	15ns	PDIP, CDIP, SOJ
MT5C6405	16K X 4 $\overline{\text{OE}}$	15ns	PDIP, CDIP, SOJ
MT5C6406/7	16K X 4 s. I/O	15ns	PDIP, CDIP, SOJ
MT5C6408	8K X 8	15ns	PDIP, CDIP, SOJ, LCC
MT5C1601	16K X 1	15ns	PDIP, CDIP, SOJ
MT5C1604	4K X 4	15ns	PDIP, CDIP, SOJ
MT5C1605	4K X 4 $\overline{\text{OE}}$	15ns	PDIP, CDIP, SOJ
MT5C1606/7	4K X 4 s. I/O	15ns	PDIP, CDIP, SOJ
MT5C1608	2K X 8	15ns	PDIP, CDIP, SOJ

*Slower speeds also available.

MICRON

TECHNOLOGY, INC.

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INTEL FROM HAMILTON/AVNET

Evaluate the **high-performance, 32-bit, 80960KB processor** quickly and cost-effectively with Intel's QT960 evaluation and prototyping boards.

The 20MHz, 80960KB delivers up to 10 VAX MIPS with burst rates of up to 20 MIPS; and has an integrated Floating Point Unit capable of over 5,000,000 Whetstones per second.

Ideal for high-performance, embedded applications, QT960 products feature a prototyping area for fast custom design; public domain design for reduced time to market; various memory configurations and an onboard debug monitor.

Compatible with a wide variety of hosts via a serial link, the QT960 boards utilize several popular Intel components, such as a 20MHz, 80960KB processor, 27C202 fast EPROMs (found in the F20 board only), 28F256 flash memory, 82380 peripheral and 82510 serial controller.

Cut through the time and expense of conventional board design with Intel's QT960 evaluation and prototyping boards from Hamilton/Avnet. For the location nearest you, call toll free, **1 (800) 442-6458**.

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- ☐ Please rush me my high-speed, EVQT960F20 Evaluation and Prototyping Board for \$1960*, which includes Intel's 27C202 fast EPROMs. I will also receive a coupon that entitles me to a 20% discount on a 80960 Development Tools Kit.
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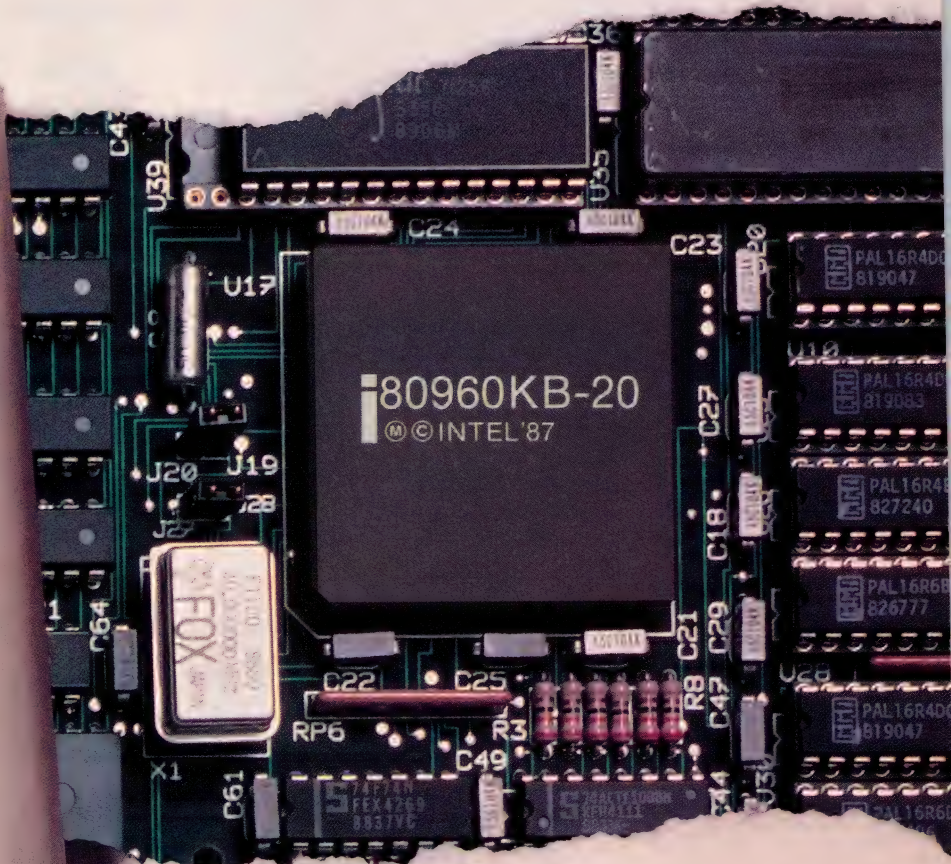
APPLICATION _____

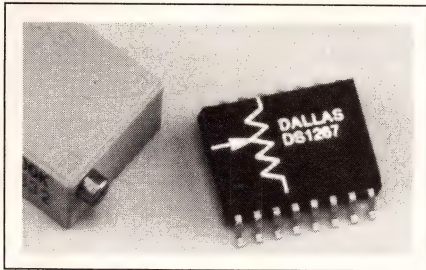
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TEAR UP THE HIGH COST OF DESIGN DEVELOPMENT





DUAL POTENTIOMETER

- Provides digital control
- Contains two 256-position controls

The DS1267 digital potentiometer contains two 256-position control elements that can be stacked for double precision, creating a dual potentiometer with 512 positions. You can also daisy-chain an unlimited number of potentiometers using only three signal wires. To set the equivalent of a wiper arm, the user writes an 8-bit word to an on-chip register. Because that number is stored in a read/write memory, you can read the settings electronically. A serial port provides the means for setting and reading the potentiometers. The device can switch from one setting to another directly—it doesn't increment through every setting. \$4.60 (100).

Dallas Semiconductor, 4350 Beltwood Pkwy S, Dallas, TX 75244. Phone (214) 450-0400. FAX 214-450-0470. TWX 650-244-1669.

Circle No 393

WIDEBAND BUFFER

- Features 450-MHz bandwidth
- Has closed-loop design

Designed for use with the company's video multiplexers and switches, the Si581 unity-gain buffer amplifier features a bandwidth of 450 MHz and -65-dB distortion at 20 MHz. The buffer's closed-loop design uses current feedback to achieve high accuracy. In the dc to 50-MHz range, the gain flatness of the Si581 is 0.5 dB max. Differential-gain and differential-phase specs are typically 0.1% and 0.01°, respectively. With a 2V step,

settling time to 0.2% is typically 5 nsec. Si581 in an 8-pin plastic DIP, \$10.82 (100). Delivery, four to eight weeks ARO.

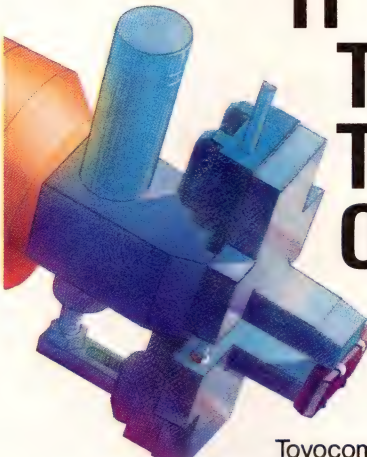
Siliconix Inc., 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (800) 554-5565; in CA, (408) 988-8000.

Circle No 394

SERIAL EEPROMS

- Have password read/write protection
- Capable of 10,000 write/erase cycles

The CAT35C704 and CAT35C804 are password-protected serial EEPROMs that allow the user to limit access to stored data via a



IT TOOK TOYOCOM TO PUT CLOCK OSCILLATORS ON TOP

Toyocom Surface Mount
Clock Oscillators

Toyocom produces crystal clock oscillators to meet the variety of surface mount applications in use today.

Now you can take advantage of tape/reel loading, and automated placement & insertion of clock oscillators, with Toyocom quality.

Used by leading electronics manufacturers around the world, Toyocom SMD's feature the exacting specifications, equivalency, and high performance today's board level designers demand.

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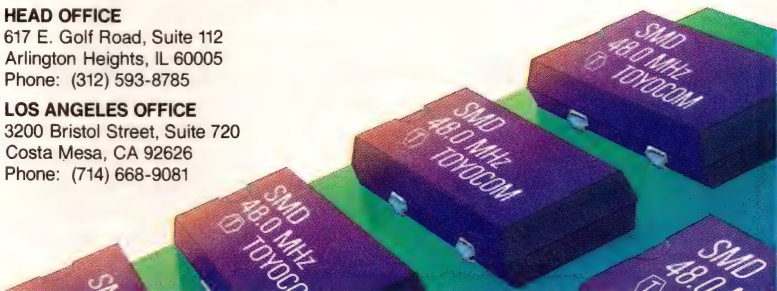
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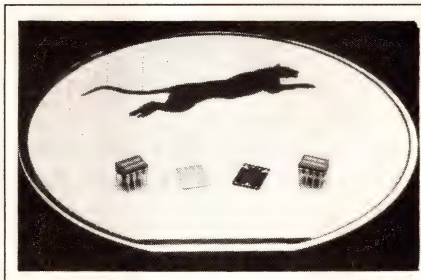
HEAD OFFICE
617 E. Golf Road, Suite 112
Arlington Heights, IL 60005
Phone: (312) 593-8785

LOS ANGELES OFFICE
3200 Bristol Street, Suite 720
Costa Mesa, CA 92626
Phone: (714) 668-9081



CIRCLE NO 23

highly secure access-control feature. You can configure both devices as either 512×8 -bit or 256×16 -bit memories and guarantee 10-year min data retention and 10,000 write/erase cycles. The 35C804 differs from the 35C704 only in its onboard UART for data transfers to 9600 baud. The 35C704 uses



a synchronous, high-speed communications protocol. The EEPROMs provide two operating modes: unprotected and password protected. In the protected mode, the access code can be 1 to 8 bytes long and can provide as many as 1.86×10^{19} combinations. CAT35C704, \$16; CAT35C804, \$18 (100).

Catalyst Semiconductor Inc., 2231 Calle De Luna, Santa Clara, CA 95054. Phone (408) 748-7700. FAX 408-980-8209. TWX 510-601-7631.

Circle No 395

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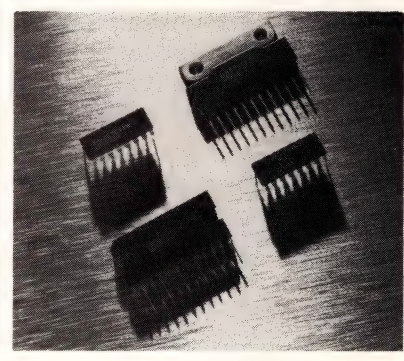
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POWER DRIVERS

- Voltage ratings from 40 to 60V
- Current ratings from 0.9 to 3.5A

Designed to drive solenoids and stepper motors, the SG3663's dual outputs are rated at ± 3.5 A peak and 50V breakdown. Internal clamp diodes provide transient suppression with inductive loads. You can configure the output stage to drive two separate loads or a single load in an H-bridge configuration. An internal sense comparator controls current in the load and features a variable threshold and hysteresis. The SG3663 comes in two different power SIPs. A second device, the SG3645, is a quad 2.5A (3.5A peak) driver with a voltage rating of 60V. Each channel consists of TTL-compatible inputs and open-collector Darlington outputs with clamp diodes. All four inputs can be enabled or disabled simultaneously through a common pin. The SG3645 comes in a 16-pin batwing DIP and a 20-

INTEGRATED CIRCUITS

pin batwing SOIC. The third device, the SG3700 dual-hammer driver, has a current rating of 900 mA and can handle output voltages to 40V. SG3663, \$4; SG3645, \$2.50; SG3700, \$2 (100). Delivery, 45 days ARO.

Silicon General, 11861 Western Ave, Garden Grove, CA 92641. Phone (714) 898-8121.

Circle No 396

WIDEBAND OP AMP

- Has 200-MHz bandwidth
- Features low-noise operation

In addition to its gain-bandwidth product of 200 MHz, the OP-61 op amp also features a low noise voltage of 3.4-nV/√Hz at 1 kHz. Other specs include an open-loop gain of 400V/mV and a typical offset voltage of 200 μV. These features ensure high performance in applications that require good dc specs, gain linearity, and wideband operation. In addition, the high slew-rate (40V/μsec max), fast settling time (330 nsec to 0.01%), and wide bandwidth provide excellent performance for high-speed signal conditioning and pulsed RF amplifiers. The OP-61 is available in 8-pin ceramic and plastic DIPs, and a 20-pin LCC. Industrial grade, from \$4.25; military grade, from \$15.80 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408)727-9222. FAX 408-727-1550.

Circle No 397

TRANSCEIVERS

- Single- and dual-channel versions
- Meet MIL-STD-1553A/B standards

The UT63M100 Series of monolithic transceivers are complete transmitter and receiver pairs conforming to MIL-STD-1553A and 1553B. The series is fully compatible with industry-standard 63100 devices. Transmit and receive data inter-

faces are TTL compatible, and idle-high and idle-low encoder/decoder interfaces are available. The receiver sections are compatible with MIL-STD-1553 levels at 0.86 to 14V. Because all necessary components are integrated onto a single die, the reliability of the UT63M100 Series is higher than comparable

hybrid devices. Pin-compatible packaging is available for designs requiring direct plug-in replacement of standard UT63M100 Series devices. For new designs, SO surface-mount packages are available. The transceivers are screened to MIL-STD-883 and are specified over the -55 to +125°C tempera-



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- (Pictured Above)
- Switches at 60 to 300 KHz
- Input Range AC 85-132V
- 30, 50, 70W Triple Output
- Safety: UL, CSA
- EMI: FCC Class "B"

MRE Series

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- Safety: UL, CSA, TUV
- EMI: FCC/VDE 0871 Class "B"

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ture range. Single-channel units, from \$236; dual-channel units, from \$367 (100).

United Technologies Microelectronics Center, 1575 Garden of the Gods Rd, Colorado Springs, CO 80907. Phone (800) 645-8862; in CO, (719) 594-8259.

Circle No 398

MICROCONTROLLER

- *Contains ADC and PWM functions*
- *Available in ROM and EPROM versions*

A member of the 80C51 family, the 87C752 is the only 28-pin microcontroller with an A/D converter and pulse-width-modulation functions on chip. Fully software compatible with the 80C51, the 87C752 contains a 5-channel ADC with a conversion time of 40 μ sec and a resolution of 8 bits. Also included are in-

put multipliers and a S/H circuit. You can use the PWM for motor and lamp control, and audio-tone generation. By disabling its output, you can also use the PWM system as a timer. The device's I²C serial-interface port allows simple connection to a variety of I²C peripheral devices ranging from EEPROM and static RAM messages to LCD drivers and clock calendars. ROM mask version, \$3; one-time-programmable EPROM version, \$10; user-erasable quartz-windowed EPROM version, \$35.

Signetics, Box 3409, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No 399

MMIC ATTENUATOR

- *Works from dc to 18 GHz*
- *Has low insertion loss*

The HMR-11000 is a GaAs monolithic-microwave IC pi-type attenu-

ator that is usable from dc to 18 GHz. Unlike PIN (positive intrinsic negative) diodes, which are current controlled, the HMR-11000 is a voltage-controlled device that uses much less power. Maximum current drain for the HMR-11000 is only 60 μ A. The device has a typical insertion loss of 2.0 dB at 12 GHz. The maximum linear attenuation is 35 dB at 2 GHz and 15 dB at 18 GHz. The analog control capability of the attenuator allows any setting within the attenuation range. Adjustment of the shunt-arm control voltage lets you use the HMR-11000 in non-50 Ω systems. The device's separate input and output control pads help provide better isolation and gain/phase dispersion. \$12.30 (1000).

Harris Semiconductor, Box 883, Melbourne, FL 32901. Phone (407) 724-3800.

Circle No 400

Do-it-yourself

Today there remains an inherent tendency to make do with "off-the-shelf" resistor networks. A designer who thinks this way, without investigating the facts, does a disservice to the design. Reduce the time to decide the proper electrical and economical solution, by deploying our Erisistor PC-program. Now, one can not only do the design, but also get price indications and delivery information. Let us show you how easily it can be accomplished.

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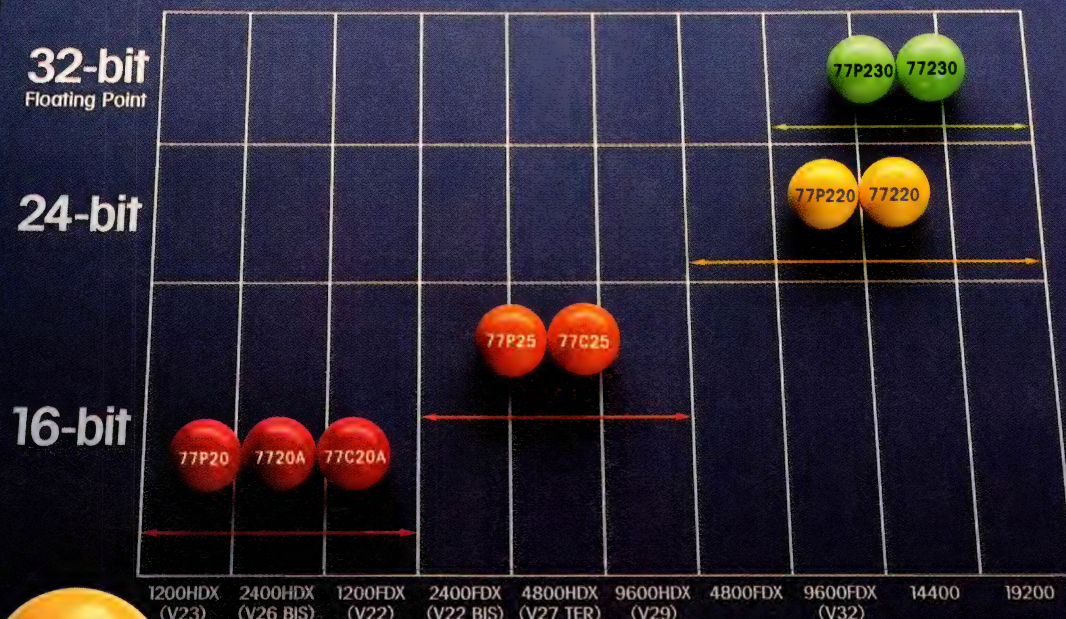
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The μ PD77220 is engineered for the V.32 specs of 9,600 bps modems. In crucial areas such as speed and efficiency, it delivers everything your high-end modem demands.

The 77220 executes all instruc-

tions in 122ns. It gives you extensive memory capacity on-chip: 2K x 32 instruction ROM, 1K x 24 data ROM, and two sets of 256 x 24 data RAM.

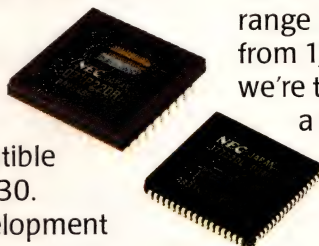
Other 77220 features include:

- ☐ EPROM version (μ PD77P220).
- ☐ Pin- and software-compatible with 32-bit 77230.
- ☐ Uses same development

tools as 77230.

- ☐ Package options: 68-pin PGA and 68-pin PLCC.

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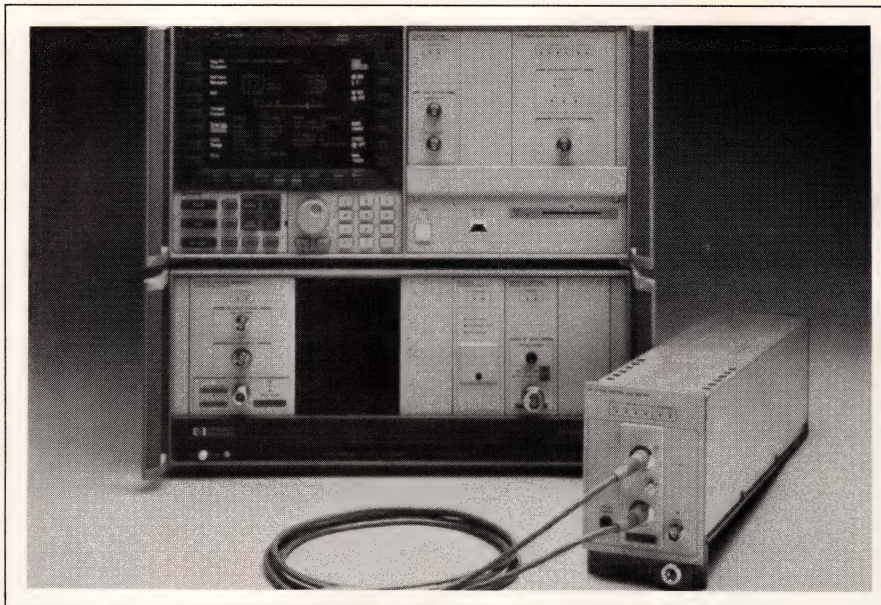
NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

SPECTRUM ANALYZER

- Provides color display and allows color printouts
- Modular construction tailors performance to your application

The HP 71000C Series of modular spectrum analyzers consists of four models. All units are built around a mainframe that includes four slots for measurement modules, a color display, and a keyboard that provides 1-key access to commonly used measurement functions. The keyboard also lets you define keystroke sequences that you can invoke with a single keypress. You can obtain color printouts of screen displays using the vendor's Paintjet printer. A data buffer permits the analyzers to continue gathering data while a printout is in progress. The analyzers have phase noise of -108 dBm at an offset of 10 kHz from the carrier. The units interface via IEEE-488 to external mass-storage devices, allowing quick

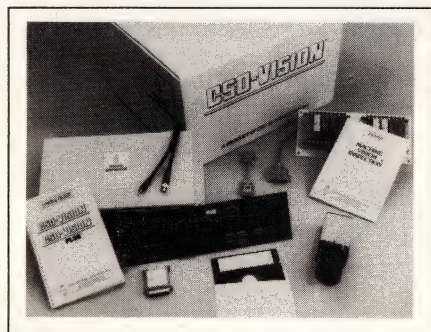


storage and recall of data, measurement setups, and user-defined menus. HP 71100C RF spectrum analyzer, \$45,000; HP 71200C microwave spectrum analyzer, \$50,000; HP 71210C high-sensitivity microwave spectrum analyzer,

\$78,000; HP 71400C lightwave spectrum analyzer, \$98,325. Delivery, 12 weeks ARO.

Hewlett-Packard Co., 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No 421



VISION SYSTEM

- Consists of hardware and menu-driven software
- Works with IBM PC, PC/XT, PS/2-30, and compatible computers

The CSD-Vision package consists of a solid-state camera with a 35-mm f/1.7 lens, a frame grabber, a VGA (Video Graphics Array) display adapter, and menu-driven software for visual inspection and picture scanning. In addition to its primary intended use in visual inspection,

the product operates as a scanner for desktop publishing. It can store images on disk in four formats. Alternative hardware and software can customize the system for specific applications. \$4995.

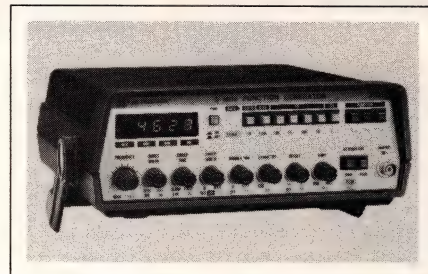
CSD International Inc., Box 10B Mohawk Trail, Shelburne Falls, MA 01370. Phone (413) 625-9736.

Circle No 422

FUNCTION GENERATOR

- Produces sine, square, and triangular waves from 0.5 Hz to 5 MHz
- Includes sweep capability and frequency counter

The 3026 sweep/function generator produces sine, square, and triangular waveforms from 0.5 Hz to 5 MHz. The unit produces continuous and gated-burst outputs. It offers variable sweep width and rate, a



ramp output to drive a scope, variable dc offset, and the ability to invert waveforms and to produce variable duty-cycle waveforms. A 3-step attenuator and a variable attenuator control the output level. A counter with four gating times and a 5-digit LED display can indicate the output frequency or the frequency of external signals to 10 MHz. \$595.

B&K Precision, 6470 W Cortland St, Chicago, IL 60635. Phone (312) 889-9087.

Circle No 423



VIBRATION CONTROL

- Provides closed-loop control for shake tables
- Supplies complex random vibration signals

The SI 1215 provides closed-loop control to complex dynamic structures that use as many as eight independent parallel channels. The modular, upgradeable unit, which supports testing in accordance with MIL-STD-810D, supplies complex random signals and can resolve 1000

discrete frequencies between 50 Hz and 10 kHz. The system includes an IEEE-488 port and two RS-423 serial ports; it can use HPGL (Hewlett-Packard Graphics Language) to control a serial-interfaced plotter. Options include a floppy-disk drive and an internal graphics strip printer. From \$24,900. Delivery eight weeks ARO.

Schlumberger Instruments, 20 North Ave, Burlington, MA 01803. Phone (800) 225-5765; in MA, (617) 229-4825. FAX 617-229-4885.

Circle No 424

8096 EMULATOR

- Supports 8098, 8095BH, 8096BH, 8097BH, 80196, and 80197 μ Ps
- Includes two 4k $\times$ 88-bit trace buffers

The HMI-200 Series now includes an in-circuit emulator that supports the 8096 and 80196/80197 μ P fami-



lies and such devices as the 8098, 8095BH, 8096BH, 8097BH, 80196, and 80197 in both NMOS and CMOS versions. The emulator contains two 4k $\times$ 88-bit trace buffers that allow 16 external trace bits and 32 bits of time-tag data. It comes with 64k bytes of emulation memory. You can expand this RAM to 256k or 1M byte of bank-selected memory. As an option, the vendor offers its Sourcegate high-level-language debugger, which supports C, PL/M, and Pascal compilers from more than a dozen vendors. The debug-

Text continued on pg 206

Optical Encoder Breakthrough!

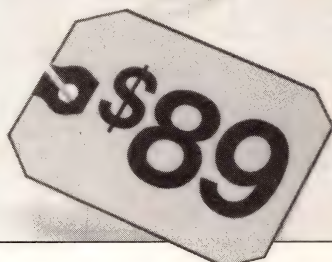
THE E20 SERIES

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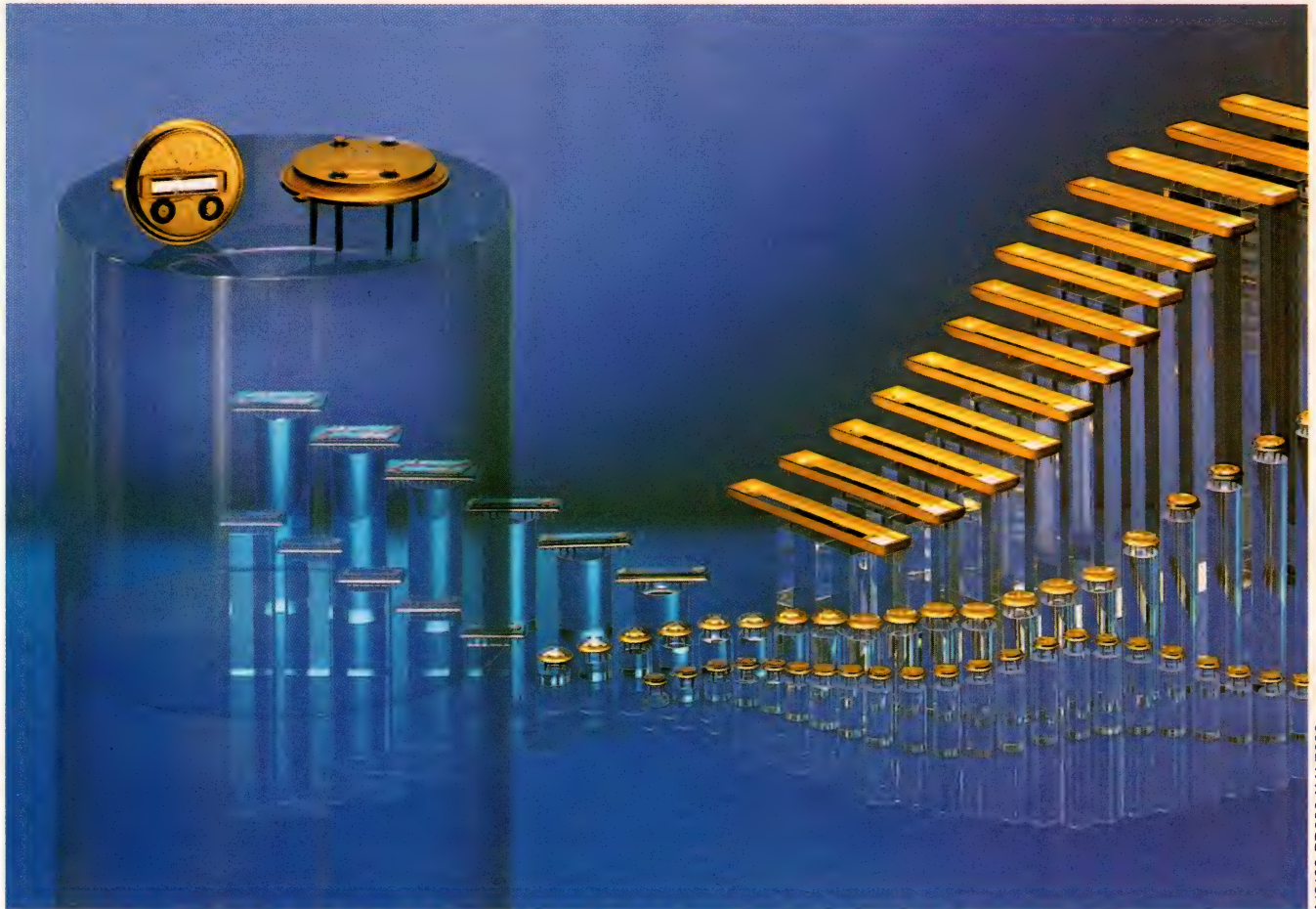
For applications that require a 26LS31 line driver, the Model E206 offers RS422 compatibility.

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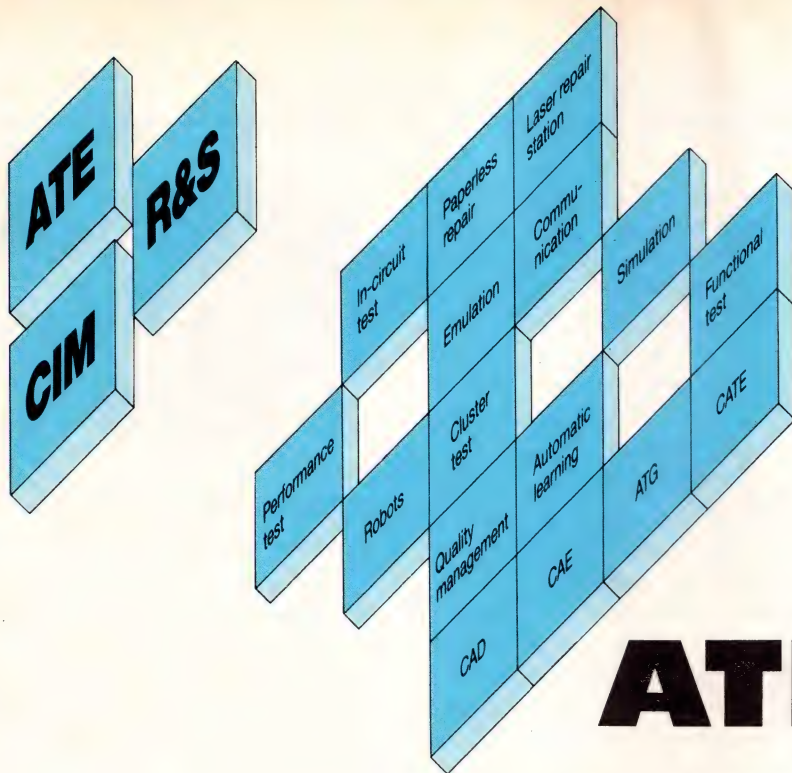
- center-frequency tolerances of ± 300 ppm with standard products and ± 50 ppm with hi-rel devices.

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ger lets you set up on-screen windows that monitor source code, assembly code, and specified memory locations. A performance-analysis option operates in real time. Emulator, \$4995; performance analysis, \$2495; debugger, \$1500 for MS-DOS and \$3000 for Sun and Apollo workstations.

Huntsville Microsystems Inc., Box 12415, Huntsville, AL 35802. Phone (205) 881-6005. FAX 205-882-6701.

Circle No 425

PLD TEST GENERATORS

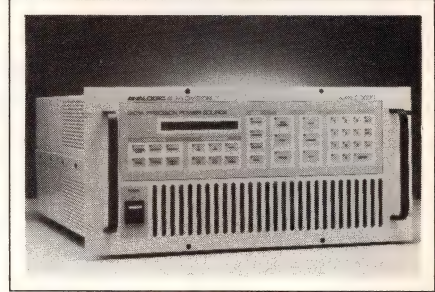
- Versions produce vectors for programmers and IC and pc testers
- \$495 entry-level package supports 23 devices with <2700 fuses

The S10, S20, S30, S31, S40, and S41 are test-vector generation software packages for PLDs. The S10 and S20 produce vectors for device

programmers. The S30 and S31 produce vectors usable on IC testers. The S40 and S41 produce vectors that work on pc-board testers. The vendor can configure the S30, S31, S40, and S41 to create vectors usable on 35 test systems. The S31 and S41 run on 80386-based computers and support devices with as many as 60,000 fuses. The computer must have 1M byte of RAM for every 6000 fuses. The other packages run on any MS-DOS-based computer with 640k bytes of RAM and support devices with as many as 6000 fuses. As with the vendor's earlier software, the vector sets do not require initializing or preloading the device under test. S10, \$495; S20, \$2995; S30 and S40, \$4995; S31 and S41, \$6995.

Anvil Software, 427-3 Amherst St, Suite 391, Nashua, NH 03063. Phone (603) 891-1995.

Circle No 426



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- Supply single-phase power to 4.5 kVA; 3 phase to 13.5 kVA
- Include waveform generator and storage for 64 waveforms

The 3100 Series precision ac power sources are intended for testing line-operated power supplies. The sources furnish as much as 4.5 kVA to single-phase loads and 13.5 kVA to 3-phase loads. The units include a waveform generator that allows you to create custom waveforms by defining sequences of preprogrammed waveforms. A high-speed

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3H Industries, 1701 Rollins Rd, Burlingame, CA 94010. Phone (415) 692-8001. FAX 415-692-8044.

Circle No 427



EMULATION TOOLS

- Support Intel, Motorola, AMD, Siemens, and Fujitsu μ Ps
- Run on IBM PCs and the vendor's 9000 Series 300 computers

The HP 64700 Series μ P development tools now support 45 members of the 8051 family, including CMOS versions, from Intel, AMD, Siemens, and Fujitsu. The emulator supports real-time, zero-wait-state program execution to 12 MHz. Its 128k bytes of dual-port emulation memory cover the full program and data space. The emulator can be hosted by an IBM PC or compatible computer or by an HP 9000 Series 300 machine. Emulation for the Motorola 68HC000 in either DIP or pin-grid packages now runs at 16 MHz with either 128k or 512k bytes of emulation memory. Owners of the vendor's older 12-MHz emulators can upgrade. The HP 64000-UX emulator, which is hosted by an HP 9000 Series 300 computer, now supports the 80386 μ P at 20 MHz with one wait state or at 16 MHz with zero wait states. 512k bytes of emulation memory is mappable over the 386's 4G-byte address

space in 256-byte increments. 8051-family tools, \$13,975 to \$16,675; 68HC000 emulation subsystems, \$14,350 to \$23,250; 80386 emulation subsystems, \$22,500 to \$26,800.

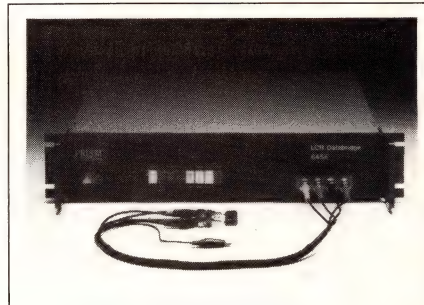
Hewlett-Packard Co., 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No 428

LCR BRIDGE

- Measures L, C, R, D, and Q to 0.1%
- Operates at 14 Hz, 100 Hz, and 10 kHz

The 6458 LCR bridge measures inductance (L), capacitance (C), resistance (R), dissipation factor (D), and quality factor (Q). The 19-in.-wide unit is 3½ in. high. The vendor supplies it with either front or rear test connections. The unit performs measurements at 14 Hz, 100 Hz,



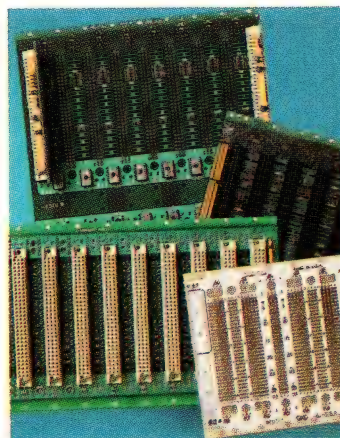
and 10 kHz and presents the results on a 5-digit high-brightness display. It can make 4-terminal measurements and includes a 2V bias source and a capacitance zero feature to offset stray capacitance. Accessories include a logging and analysis software package for IBM PCs. £1295.

Prism Electronics Ltd, Burrell Rd Industrial Estate, St Ives, Huntingdon, Cambridgeshire PE17 4NF, UK. Phone (0480) 62225. FAX 0480-494047.

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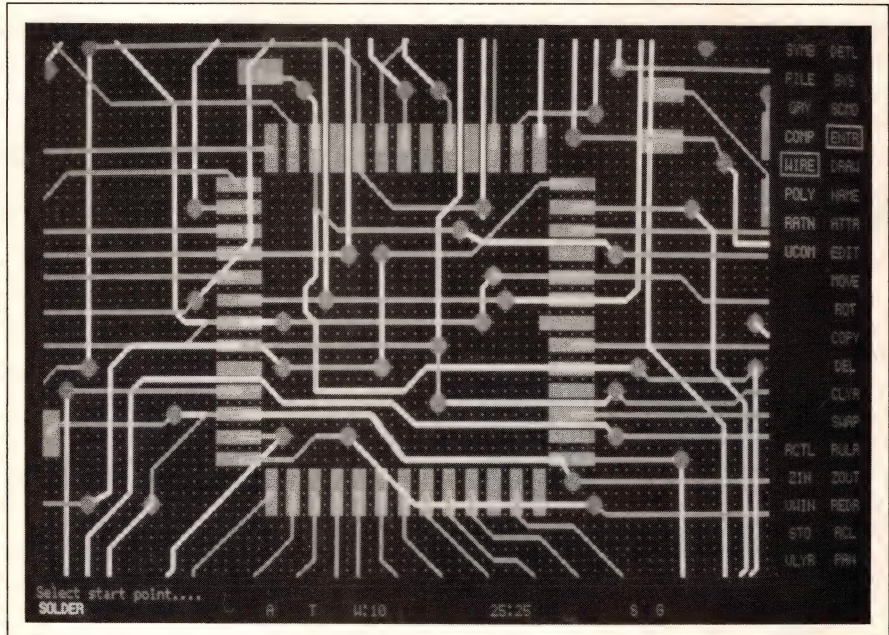
NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS

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- Can route all layers or any pair of layers at one time
- Handles SMT designs

Rip-N-Route gives you precise control of routing strategies and includes an optimizer to guarantee maximum manufacturability. The router is fully compatible with the vendor's Master Designer product. You can at one time route any pair of layers together or all layers simultaneously. In addition, you can confine the routing to a specified window. Automatic via fanout (stringer generation) for SMT designs can save you hours of manual editing. You can select uniform and nonuniform routing grids, separate via grids, and multiple trace widths. To maximize channel utilization, you can specify 45° beveling either during routing or as a post-process. The router is fully interruptible and re-entrant at any time during the process. The menu-driven interface allows you to cus-



tomize the routing for specific technologies and design styles; on-line help is instantly available for all menu items. The package runs on IBM PCs and compatibles. The Total Route package, which includes Autoplace, Master Router, and

Rip-N-Route, costs \$6495; Rip-N-Route is available separately as an upgrade for \$1995.

P-CAD, 1290 Parkmoor Ave, San Jose, CA 95126. Phone (408) 971-1300.

Circle No 401

VLSI LAYOUT TOOL

- Synthesizes each layout from a small set of primitives
- Can be used with any fabrication process

AutoCustom is a VLSI layout package that synthesizes each layout from a small set of primitive structures. It builds gates and other devices on-the-fly, and needs no cell library. Typical circuits are two to three times smaller than equivalent circuits implemented with standard cells, thereby reducing chip area and cost. The technology also reduces crosstalk and increases immunity to latchup. Because the layouts are scalable, you can use the package with any fabrication process once you have entered the appropriate process parameters and design rules. The package currently runs on Apollo Domain workstations and

costs \$4995; other versions for Sun workstations and 80386-based machines are in preparation.

Integrated Circuit Technology Inc., 22691 Lambert St, Suite 514, El Toro, CA 92630. Phone (714) 581-7195. FAX 714-581-7196.

Circle No 402

ASIC SIMULATOR

- Provides logic and fault simulation for cells and gate arrays
- Runs on Mach 1000 hardware accelerator

The Necsim system provides accelerated logic and fault simulation for ASIC design and verification. The system can handle a wide variety of complex standard cells and gate arrays and, because it runs on Zycad's Mach 1000 accelerator, the simulations run much more quickly

than they would on mainframes or larger workstations. The system works with the vendor's 1.2- and 1.5- μ m CMOS libraries, and you can use it to qualify new products, including the vendor's advanced ECL and BiCMOS arrays. \$23,800 per site.

NEC Electronics Inc., Box 7241, Mountain View, CA 94039. Phone (415) 960-6000. TWX 910-379-6985.

Circle No 403

PC DIAGNOSTIC TOOL

- Automatically identifies processor and type of bus
- Includes hardware checks and low-level formatter

The QAPLus is a menu-driven diagnostic tool for IBM PCs, PS/2s, and compatibles. One version runs on all systems and automatically iden-

CAE & SOFTWARE

tifies the processor and bus type, as well as the presence or absence of a math coprocessor. The hardware-configuration checks report the amount of base, extended, and expanded memory; the video mode you're running; and the capacity of all floppy and hard disks. The CPU test checks the processor, DMA/Micro Channel Architecture (MCA) channels, interrupt controllers, clock/calendar operation, and the protected mode of operation on 80286- and 80386-based systems. The memory test provides a wide variety of write patterns to ensure that all memory errors are found, including parity errors and bent pins; the report explicitly identifies each bad chip. Other tests include a keyboard test (including mouse and joystick tests), a video test, and a low-level hard-disk formatter that allows you to select the interleave interval and to edit bad-track tables. Benchmarks report CPU performance (in Dhrystones), math performance (in Whetstones), system speed (in megahertz), and video performance. The program reports all errors in English (not numeric codes) and suggests the most likely causes of each error. \$134.95.

DiagSoft Inc., 6001 Butler Lane, Scotts Valley, CA 95066. Phone (408) 438-8247. FAX 408-438-7113.

Circle No 404

Z8 DEBUGGER

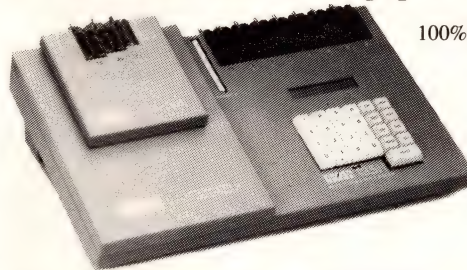
- Lets you debug Z8 code on an IBM PC
- Handles both C and assembly-language source code

The Micro/SLD-Z8 symbolic debugger executes Z8 machine code on an IBM PC or compatible development host. The built-in simulator means that you don't need any additional hardware, such as the target system or an in-circuit emulator, to debug your programs. You can step through programs written in C or assembly-language (or a combina-

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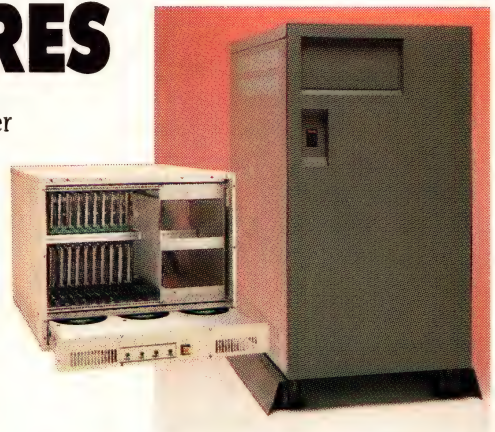
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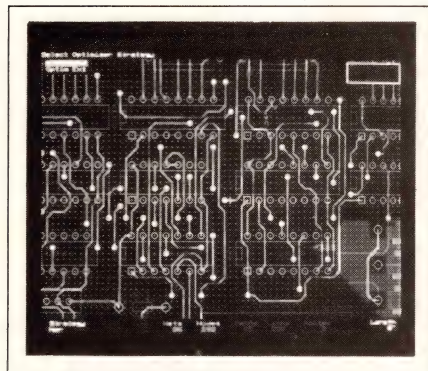
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CIRCLE NO 29

tion of both) line by line, or run at full speed until the debugger encounters a breakpoint in the code or data. Separate windows display the source code as well as the contents of Z8 hardware registers and data variables stored in memory. The debugger works with the vendor's Micro/C cross-compiler and assembler package, or with any assembler that can generate output in Intel Hex format. The debugger supports 19 versions of the Z8, including CMOS parts, and handles all on-chip devices such as the UART, timers, and interrupt controller. \$295.

Micro Computer Control Corp., Box 275, Hopewell, NJ 08525. Phone (609) 466-1751. FAX 609-466-4116.

Circle No 405



BOARD-LAYOUT TOOL

- *Enhancements double the number of ICs and pads you can use*
- *Provides track and vias optimization*

PCB II is a greatly enhanced version of the vendor's PCB board layout tool. A new, user-definable, memory-allocation system lets you include as many as 270 (instead of 130) ICs and 6000 (instead of 1850) pads in your design, all within 640k bytes of RAM. The package permits manual routing, but a new analysis and rip-up rerouting feature optimizes track placement and minimizes the number of vias in your pc-board design. The documentation has been completely re-

vised, and now includes updated tutorial material and additional reference sections. A comparison feature lets you check your final net list against the net list generated by the vendor's schematic-capture program. The enhanced version also includes expanded drill-template capabilities. \$1495.

OrCAD Systems Corp., 1049 SW Baseline St, Suite 500, Hillsboro, OR 97123. Phone (503) 640-9488. FAX 503-640-6491.

Circle No 406

CAD FOR MACINTOSH

- *Maintains a hierarchy of schematic block diagrams*
- *Rule checking ensures consistency*

Macstile is a schematic-capture and system-design tool that runs on the Macintosh personal computer. The package maintains a hierarchy of schematic block diagrams called "blueprints," each of which describes how a component is constructed from other components. Associated text can record design decisions and other important details of implementation. The program is menu-driven and can support a variety of design methodologies, including object-oriented design, structured design, flowcharts, control-system block diagrams, and logic design. \$199.

Software Originals Inc., 5442 Monroe St, Toledo, OH 43623. Phone (419) 885-8747.

Circle No 407

LANGUAGE TRANSLATOR

- *Translates from any programming language to any other*
- *Lets you implement compilers, assemblers and macroprocessors*

Metamorphosis is a generic computer program that runs on IBM PCs and compatibles that have at least 416k bytes of RAM and two disk drives. When given files containing the syntactical definitions of

a source language and a target language, the program can translate programs written in the source language to functionally identical programs written in the target language. You can use the generic version to implement compilers, assemblers, macroprocessors, and query-language processors; to reformat character-oriented database files; to analyze grammar and to analyze and convert sequential to parallel procedures; and to perform many other conversion tasks. In addition to the generic version (\$387), you can obtain three prepackaged translators to convert from Fortran IV to C (\$87), from PL/I (Subset G) to C (\$87), and from CMS-2M to Ada (\$134).

Shannon Associates Inc., Box 597, Chapel Hill, NC 27514. Phone (919) 929-6863.

Circle No 408

THERMAL ANALYZER

- *Lets you locate hot spots in your design*
- *Model accounts for voids in solder between two layers*

Thermal Analysis—a software package that runs on IBM PCs and compatibles—allows you to perform thermal analysis on designs for IC hybrids, power supplies, and power hybrids. The program lets you locate potential hot spots in multichip, multilayer, and high-density packages at an early stage in the design cycle. The model also accounts for voids in the solder joining two or more layers; an option lets you take into account direct bonding. You can display the results of the analysis either as thermal resistance or as temperature contours on graphical outlines of the device under test. \$1980.

Heat Transfer Research & Development Ltd (HTRD), 1010 W Lonnquist Blvd, Mt Prospect, IL 60056. Phone (312) 577-5967. FAX 312-577-4229.

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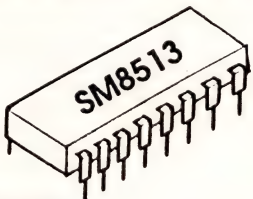
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SM8513

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For complete product information please contact Greg Branch, Sales Director.



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CIRCLE NO 31

EDN September 1, 1989

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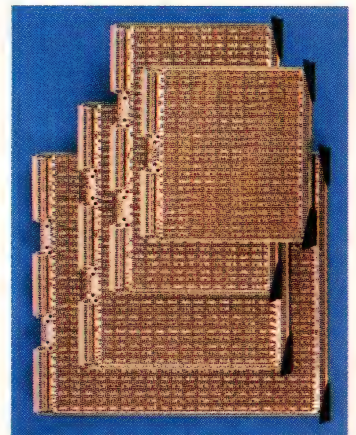
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CIRCLE NO 32

LITERATURE

Details on programming a network interface card

The vendor's application note, Ziatechniques 6, "Developing software for an Arcnet network interface," tells you how to program an Arcnet interface board. The 10-pg note contains detailed code examples and timing calculations.

Ziatech Corp, 3433 Roberto Ct, San Luis Obispo, CA 93401.

Circle No 410



How to select a DSO

This 11-minute videotape, *DSOs with a Difference*, discusses digital-storage-oscilloscope technology and the features to look for when selecting a scope. The tape focuses on the company's PM 3335/PM 3350/PM 3365 family of medium-frequency A/D storage oscilloscopes.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206.

Circle No 411

Ansys tutorials and summary available

Nine tutorials delineate the features of the Ansys program, revision 4.4, as well as the 1989 2-volume set, *Ansys Conference Proceedings*, which contains 96 of the 99 technical papers delivered at the 4th International Ansys Conference. The tutorials discuss the Ansys finite-element-analysis program, and topics include nonlinear dynamics, acoustics, a 4-node shell element coupled with field analysis,

postprocessing, and solid modeling. The conference proceedings deal with Ansys applications in the aerospace, automotive, and electronics businesses; interfaces to CAD programs; university projects; and management and legal issues. Tutorials, \$8 to \$20; entire set, \$60; proceedings, \$60.

Swanson Analysis Systems Inc, Box 65, Houston, PA 15342.

INQUIRE DIRECT

Flyer highlights token-ring analyzer

This 6-pg pamphlet provides an overview of the vendor's Interview 1000 token-ring network analyzer, which provides information on network utilization, configuration, errors, and network management. The publication shows how the analyzer can benefit you if you plan to install a token-ring local-area network.

Atlantic Research Corp, Teleproducts Div, 7401 Boston Blvd, Springfield, VA 22153.

Circle No 412

Microprocessor manual illuminates software tools

The vendor's latest user manual details software development tools for embedded microprocessor systems. The multicolor publication comes in a 3-ring binder that features pockets in the front and back for document storage.

Introl Corp, 647 W Virginia, Milwaukee, WI 53204.

Circle No 413

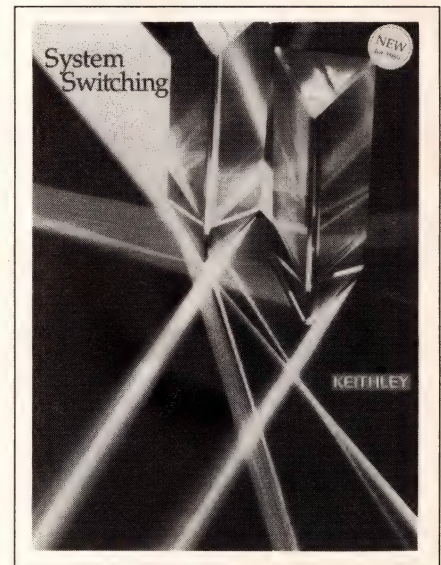
Selecting 3-D molded circuits

This 8-pg brochure, which discusses 3-D molded-circuit products, covers the vendor's complete range of related design services and production resources in the areas of molding, imaging, and plating. Applications include multiplanar circuits,

right-angle circuits, and chip-on-board and plated 3-D structures used as antennas.

ICI Electronics, Wilmington, DE 19897.

Circle No 414



Brochure presents system-switching modules

Thirty-two switching-matrix, multiplexing, and scanner modules are described in this 25-pg brochure. This publication also provides a switching-matrix-card selector guide with information about switch type, card configuration, maximum switching levels, contact potential, maximum recommended frequency, and common applications. Further, a selector guide for accessories lists connector kits, tools, and adapters, as well as other accessories, and details their applications.

Keithley Instruments Inc, 28775 Aurora Rd, Cleveland, OH 44139.

Circle No 415

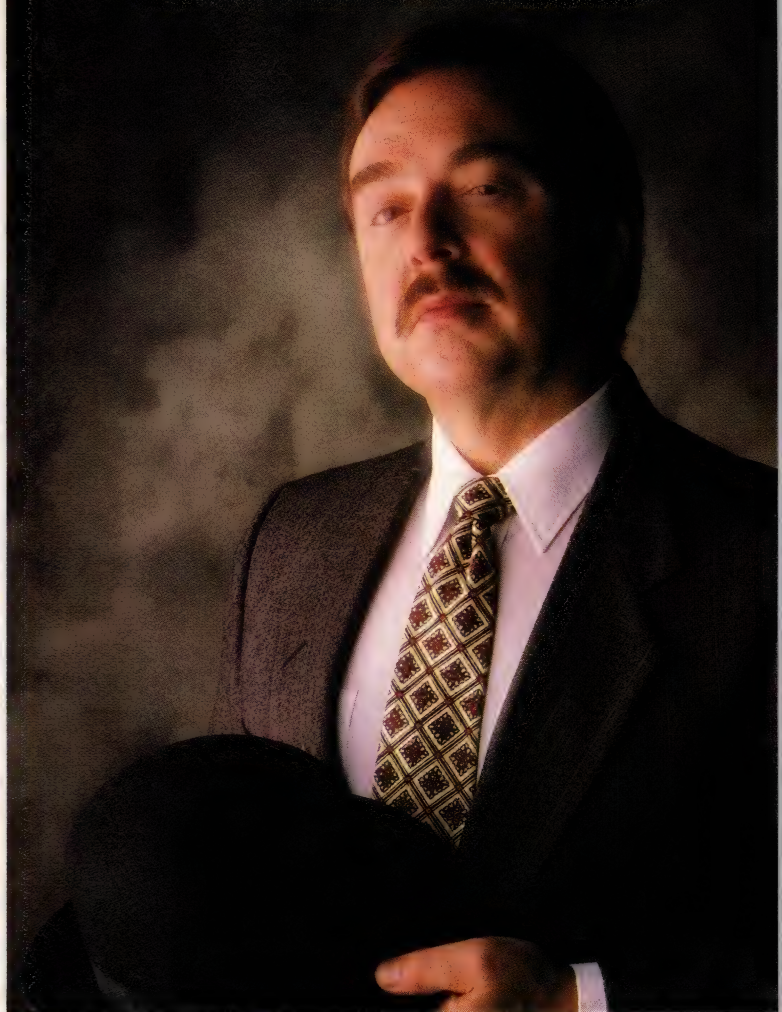
Displays of noise-figure and scalar parameters combined

A 2-pg product note (8970B/S-4) "Displaying HP 8970B Noise Figure Meter Measurements on the HP 8757 Scalar Network Analyzer," spotlights the setup, capabilities,

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and operation of the equipment. The note shows how to use the scalar network analyzer's CRT display as a plotter and how you can display gain and noise-figure data from the noise-figure meter without using other equipment.

Hewlett-Packard Co., 19310 Pruneridge Ave, Cupertino, CA 95014.

Circle No 416



Microwave-counter profile

This brochure presents the Model 2440 10-Hz to 20-GHz microwave counter, which is designed for production and maintenance in civil and military communications, radio links, and satellites. The publication covers the instrument's features and specifications. It also describes how the 2440 is designed for complex signals having high FM and AM tolerance and superior amplitude discrimination.

Marconi Instruments, 3 Pearl Ct, Allendale, NJ 07401.

Circle No 417

Pamphlet describes 12-in., 90° monitors

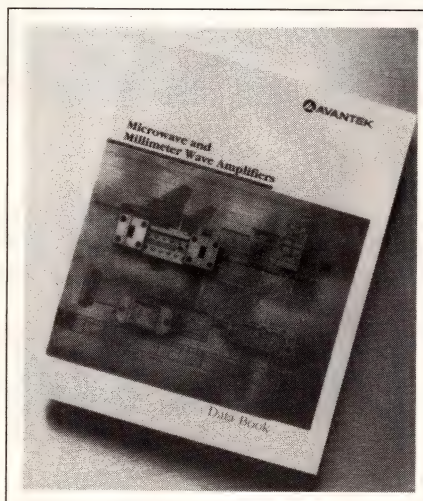
This technical brochure presents dimensions, photographs, a standard product specifications chart, and customizing options for the vendor's



12-in., 90° monochrome display monitors. The schematics and general specifications help you select the best monitor for your application.

DisplayTek Inc., 1355 Holmes Rd, Elgin, IL 60123.

Circle No 418



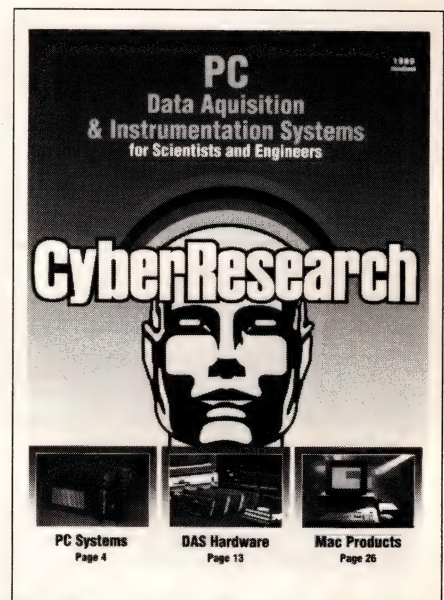
Data book of amplifiers

The 224-pg data book, entitled *Microwave and Millimeter Wave Amplifiers*, describes a complete line of military, industrial, commercial, and telecommunications microwave and millimeter-wave-amplifier products. Introduced in this issue are a line of microstrip gain modules, as well as a wide range of high-power amplifiers and millimeter-wave amplifiers operating as high as 60 GHz. Product categories include low-

noise, gain-control, and power and limiting amplifiers; millimeter-wave down-converter assemblies; and solid-state traveling-wave-tube amplifier replacements. Also covered are the vendor's transceivers, satellite earth-station amplifiers, and high-power traveling-wave-tube retrofit products for point-to-point microwave and cellular-radio base-station amplifiers.

Avantek Inc., M/S M82, 481 Cottonwood Dr, Milpitas, CA 95035.

Circle No 419



Handbook of PC systems

The 1989 *PC Systems Handbook for Scientists and Engineers* outlines recent, as well as standard, products for PC-based data acquisition and process control. Included in the book are ADCs, multiport serial boards, IEEE-488 interfaces, digital-oscilloscope boards, and PC expansion chassis for use with IBM-compatible computer systems. The write-up of recent products includes Micro Channel peripherals to use with IBM's PS/2 line; an entire section covers products that run with Macintosh II/Ix and Macintosh SE machines.

CyberResearch Inc., Box 9565, New Haven, CT 06536.

Circle No 420

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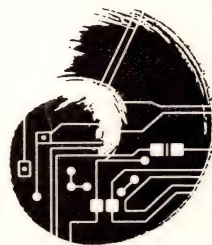


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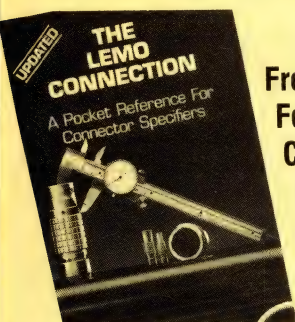
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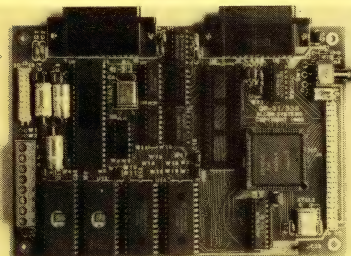
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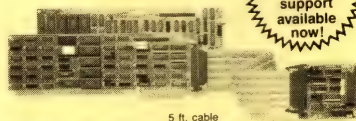
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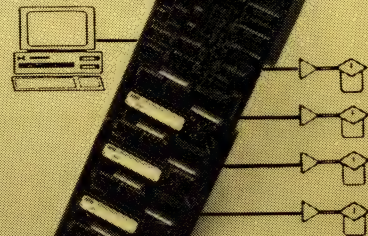
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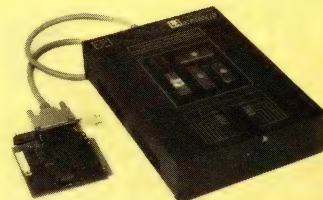


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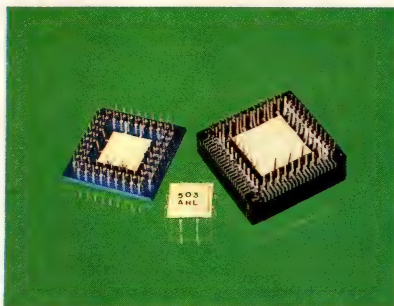
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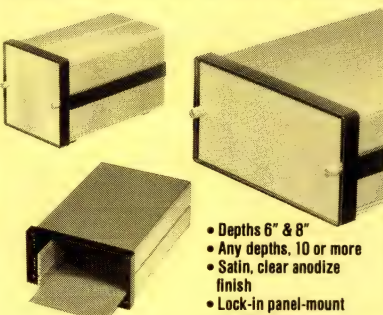
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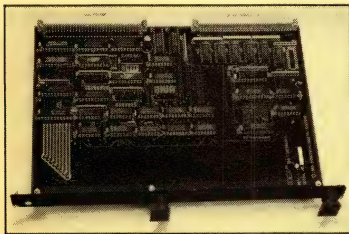
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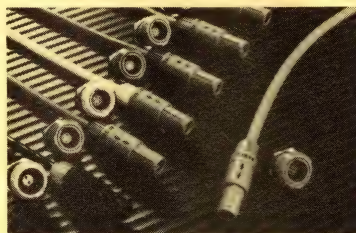


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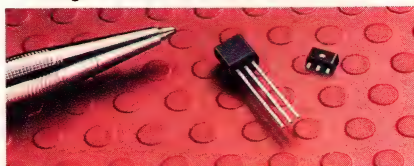
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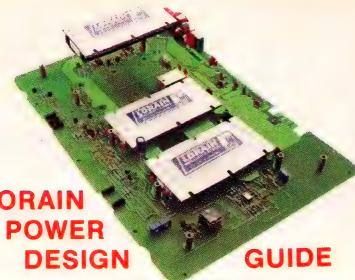
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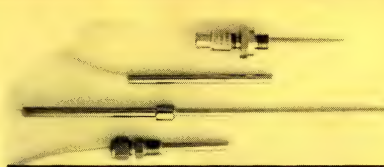
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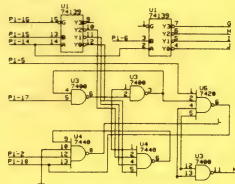


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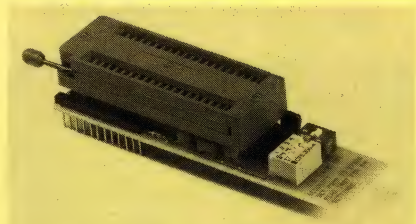


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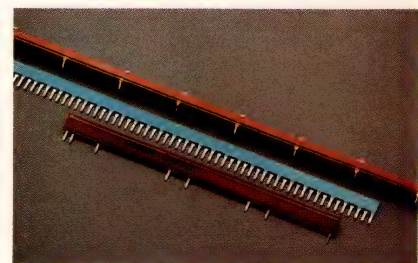
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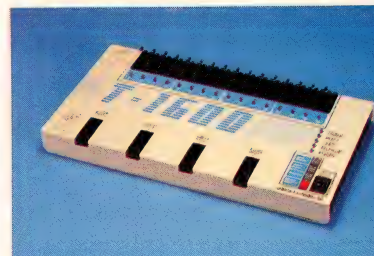
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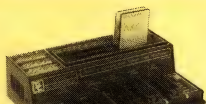


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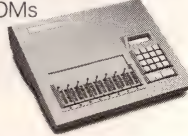
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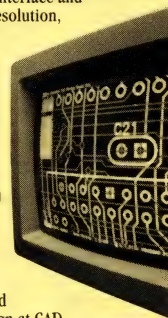
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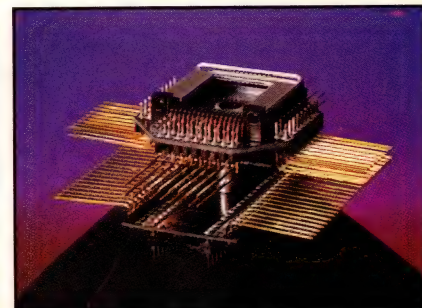
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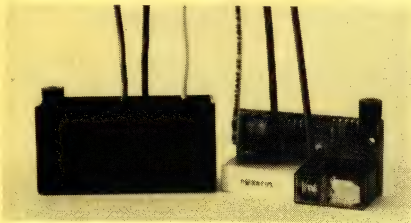
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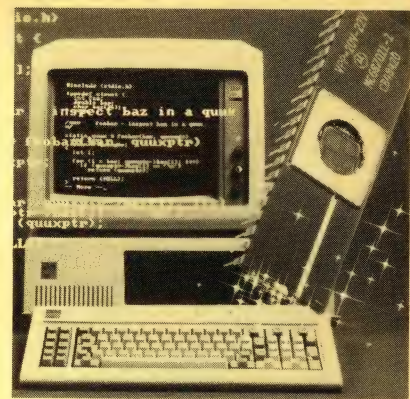
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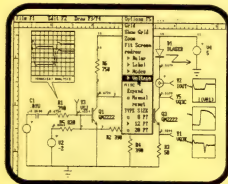
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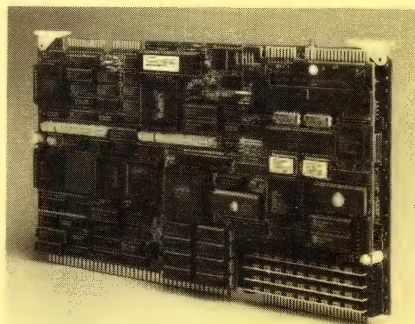
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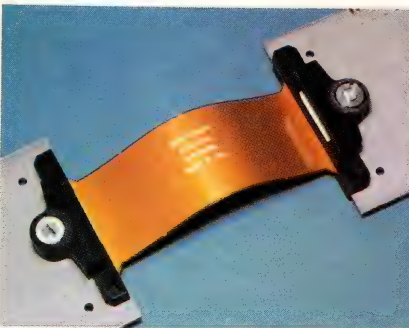


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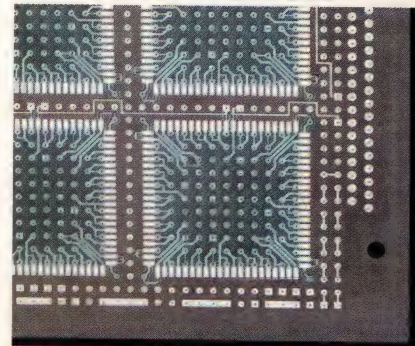
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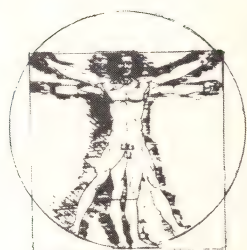
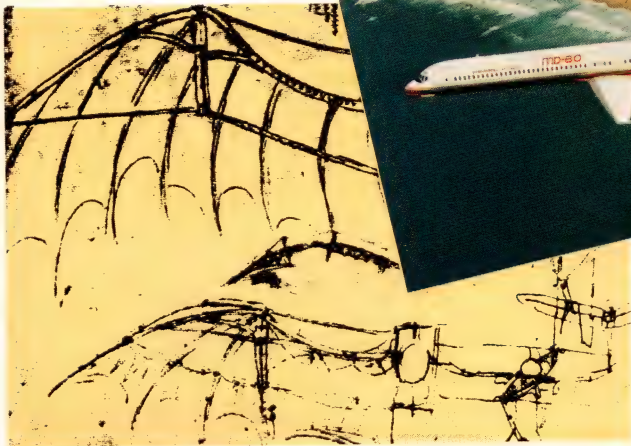
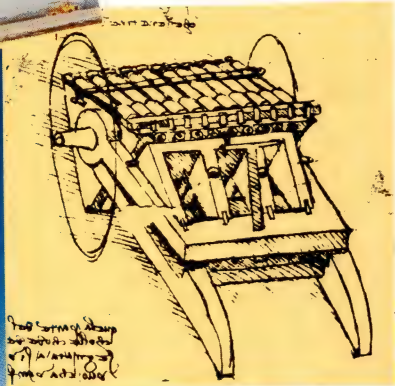
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Issue Date	Recruitment Deadline	EDN	
		Editorial Emphasis	EDN News Edition
Sept. 28	Sept. 7	Integrated Circuits, Computer Peripherals	Closing: Sept. 15 Mailing: Oct. 5
Oct. 12	Sept. 21	DSP Chip Directory, Integrated Circuits	Closing: Sept. 28 Mailing: Oct. 19
Oct. 26	Oct. 5	Test & Measurement Special Issue Computers & Peripherals	Closing: Oct. 27 Mailing: Nov. 16
Nov. 9	Oct. 19	CAE, Integrated Circuits	Closing: Nov. 9 Mailing: Nov. 30
Nov. 23	Nov. 2	16th Annual $\mu P/\mu C$ Directory, Integrated Circuits	Closing: Nov. 22 Mailing: Dec. 14
Dec. 7	Nov. 16	Product Showcase — Volume I, Power Supplies	
Dec. 21	Nov. 30	Product Showcase — Volume II, Components	

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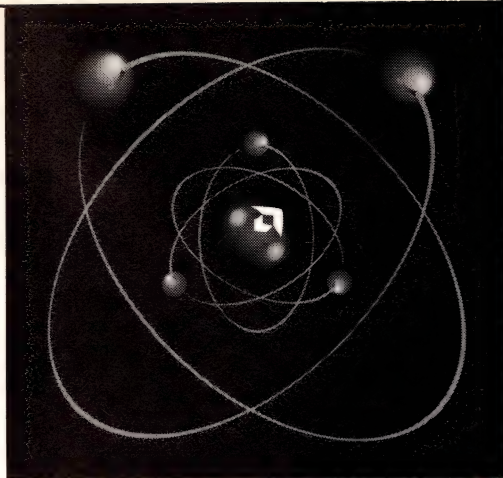
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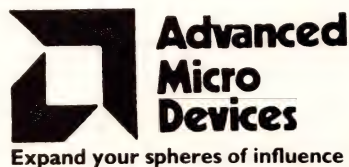
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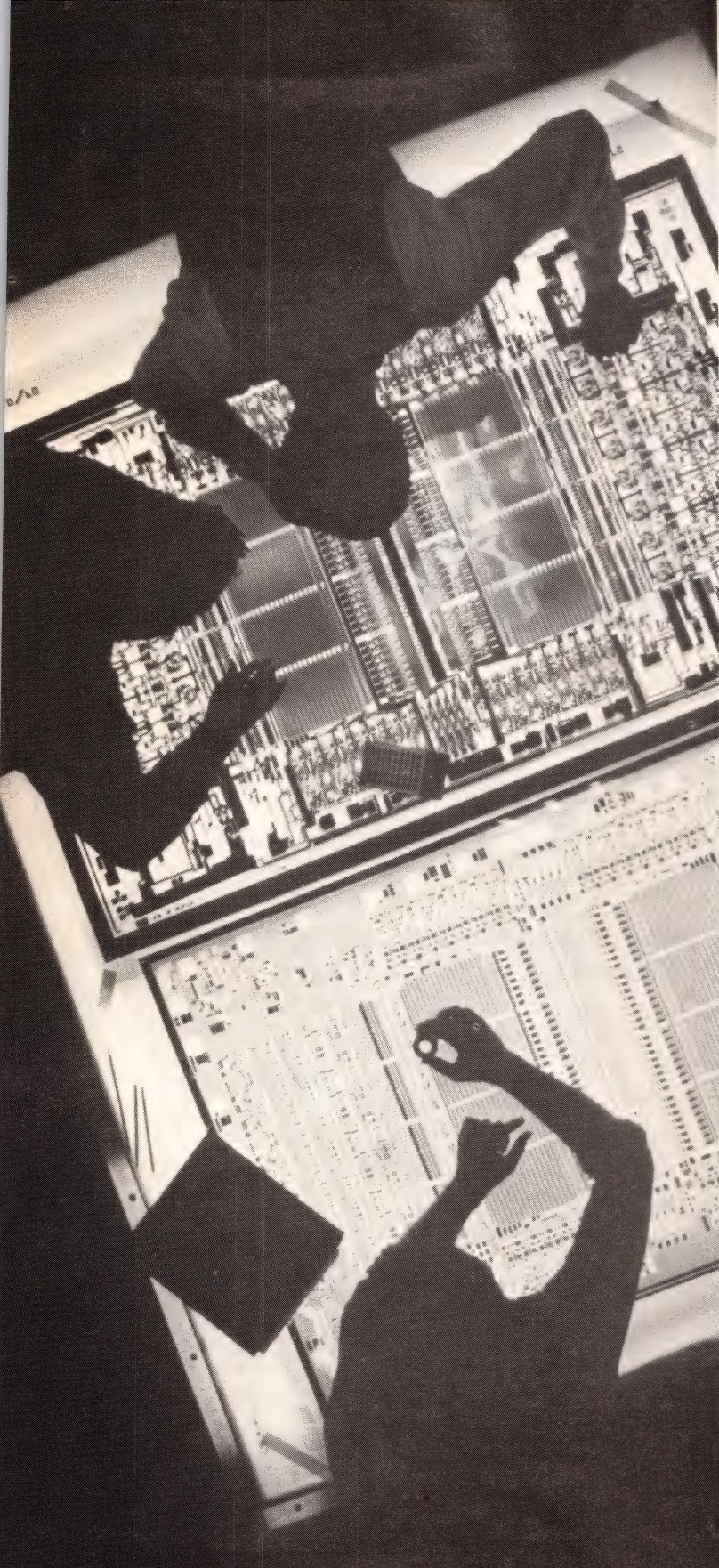
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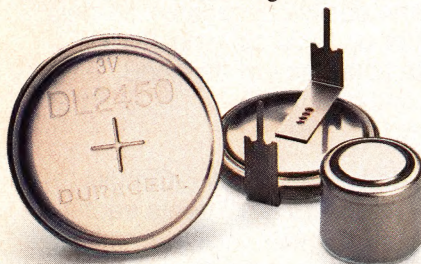
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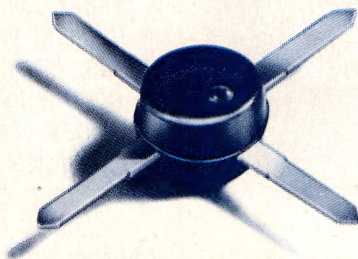
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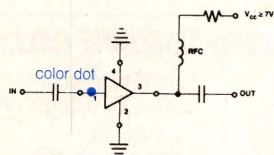
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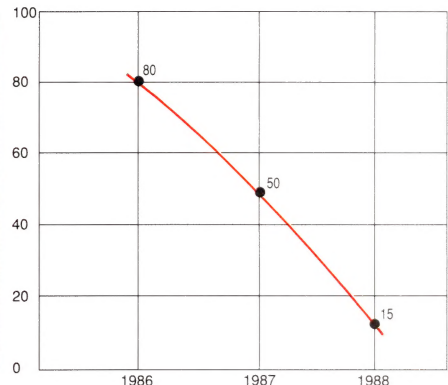
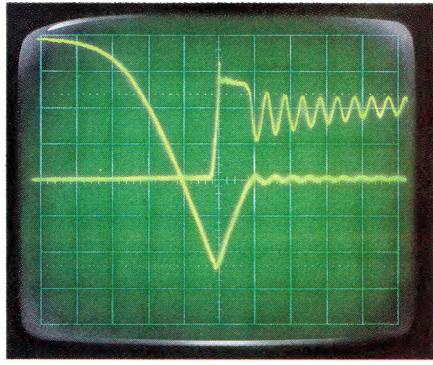
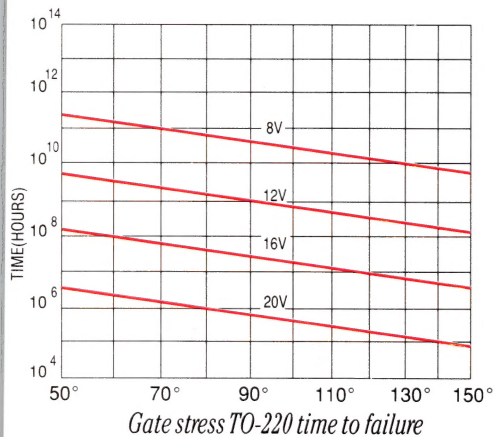
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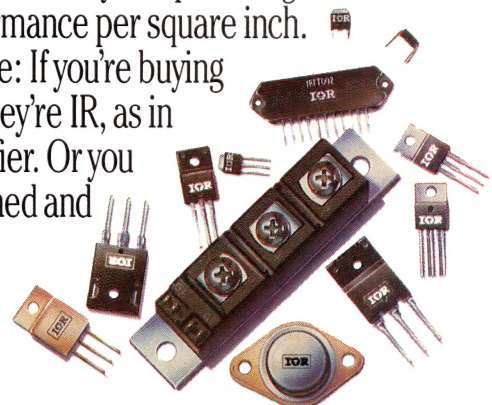
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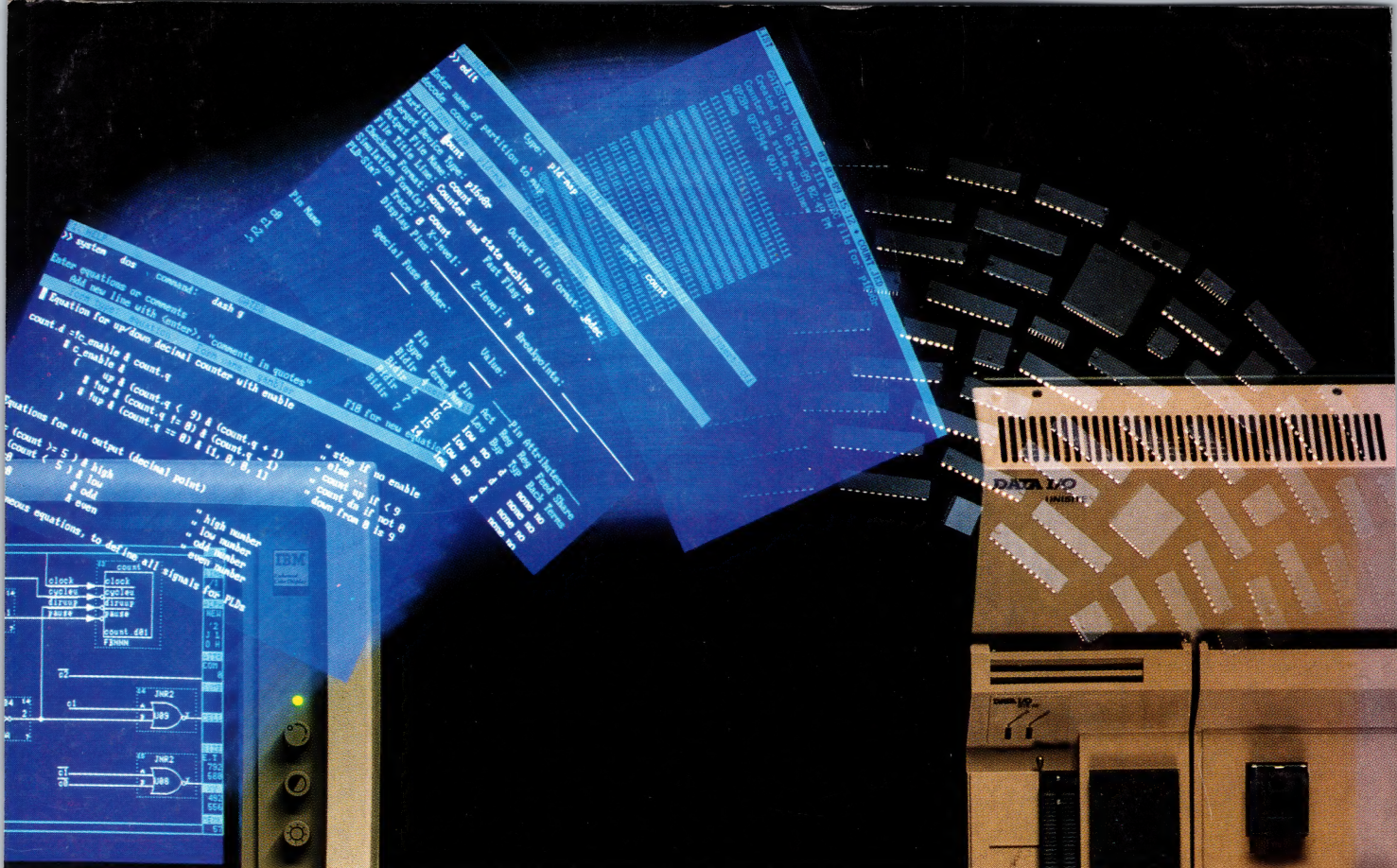
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